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High Efficiency Single Phase Transformer less PV Multilevel Inverter

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Abstract: *Renewable energy sources are getting more and more widespread, mainly due to the fact that they generate energy by keeping the environment clean. Most of these systems have an isolation transformer included, which if excluded from the system would increase the efficiency and decrease the size of PV installations, furthermore it would lead to a lower cost for the whole investment. For safety reasons grid connected PV systems include galvanic isolation. In case of transformerless inverters, the leakage ground current through the parasitic capacitance of the PV panels, can reach very high values. A common-mode model based on analytical approach is introduced, used to predict the common-mode behavior, at frequencies lower than 50kHz, of the selected topologies and to explain the influence of system imbalance on the leakage current. It will be demonstrated that the neutral inductance has a crucial influence on the leakage current. Finally simulation results will be shown for the NPC multilevel inverter topology, emphasizing the low leakage current for the case of a grid connection without galvanic isolation.*

Keywords: *Leakage current, parasitic capacitance, switching converter, NPC.*

1. Introduction

Grid connected photovoltaic (PV) systems have an important role in distributed power generation. With the help of governmental incentives their usage becomes more and more widespread within the community. According to the latest International Energy Agency Photovoltaic Power Systems (IEA-PVPS T1-15:2006) report, the annual rate of growth of the cumulative installed capacity in the IEA PVPS countries was at an impressive 42%. The PV market in Germany had a 75% growth during the year 2005 with more than 600MWp of installed capacity. [1] Most of the single-phase installations are small scale PV systems, of up to 5-6 kWp [2]-[7]. A single-phase system means that there is a pulsating AC power on the output, whilst the input is a smooth DC. Large DC capacitors are required which decrease the lifetime and reliability of the whole system.

On the other hand in a three phase system, there is constant AC power on the output, which means that there is no need for large capacitors, leading to smaller cost and a higher reliability and lifetime of the whole system. Also the power output of these systems can be higher, reaching up to 10-15 kWp in case of rooftop applications.

A single-phase grid-connected inverter is usually used for residential or low-power applications of power ranges that are less than 10 kW [1]. Types of single-phase grid connected inverters have been investigated [2]. A common topology of this inverter is full-bridge three-level. The three-level inverter can satisfy specifications through its very high switching, but it could also unfortunately increase switching losses, acoustic noise, and level of interference to other equipment. Improving its output waveform reduces its harmonic content and, hence, also the size of the filter used and the level of electromagnetic interference (EMI) generated by the inverter’s switching operation [3]. Multilevel inverters are promising; they have nearly sinusoidal output-voltage waveforms, output current with better harmonic profile, less stressing of electronic components owing to decreased voltages, switching losses that are lower than those of conventional two-level inverters, a smaller filter size, and lower EMI, all of which make them cheaper, lighter, and more compact [3], [4].

Fig. 1 has been made from the database of more than 400 commercially available PV inverters, presented in a commercial magazine about PV systems. The conclusion drawn from these graphs is that transformer less inverters have higher efficiency and smaller weight and size than their counterparts with galvanic separation.

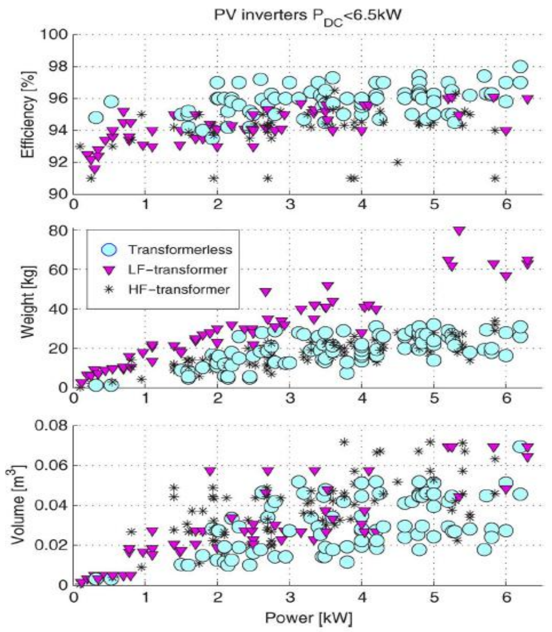

Figure 1. *Advantages and drawback of different inverter topologies.*

In order to minimize the ground leakage current through the parasitic capacitance of the PV array, several techniques have been used.

One of them is to connect the midpoint of the dc-link capacitors to the neutral of the grid, like the half-bridge, neutral point clamped (NPC), or three-phase full bridge with a split capacitor topology, thereby continuously clamping the PV array to the neutral connector of the utility grid. Half-bridge and NPC type of converters have very high efficiency, above 97%.

Furthermore, the topology proposed reduces the dc current injection, which is an important issue in the case of transformer less topologies and is limited by different standards. The non-injection of dc current into the grid is topologically guaranteed by adding a second capacitive divider to which the neutral terminal of the grid is connected. An extra control loop is introduced that compensates for any dc current injection, by controlling the voltage of both capacitive dividers to be equal.

Another solution is to disconnect the PV array from the grid, in the case of H-bridge (HB) inverters, when the zero vector is applied to the load (grid). This disconnection can be done either on the dc side of the inverter (like the topology from and H5 topology from Solar Technologies AG) or on the ac side (like the Highly Efficient and Reliable Inverter Concept (HERIC) topology from Sun ways).

A new topology called HB zero-voltage state rectifier (HB-ZVR) is given where the midpoint of the dc link is clamped to the inverter only during the zero-state period by means of a diode rectifier and one switch.

The aim of the work presented in this paper is to introduce a common-mode model based on analytical approach for the single phasephase inverter connected to the utility grid with the help of NPC multi level inverter. This model will be used to predict the common-mode behavior, at frequencies lower than 50kHz, of the selected topologies and to explain the influence of system imbalance on the ground leakage current. It will also be shown, that the neutral inductance has a crucial influence on the common mode behavior of the topology, thereby directly influencing the ground leakage current of the system. Simulation results will be presented in case of the NPC topology in order to validate the simulation model.

2. Transformer less Topology Analysis

As discussed in previous works, the common-mode voltage generated by a topology and modulation strategy can greatly influence the ground leakage current that flows through the parasitic capacitance of the PV array. Generally, the utility grid does not influence the common-mode behavior of the system, so it can be concluded that the generated common mode voltage of a certain inverter topology and modulation strategy can be shown using a simple resistor as load. Therefore, in the case of simulations, only a resistive load is used, and the common-mode voltage is measured between the dc+ terminal of the dc source and the grounded middle point of the resistor as shown in Fig. 2.

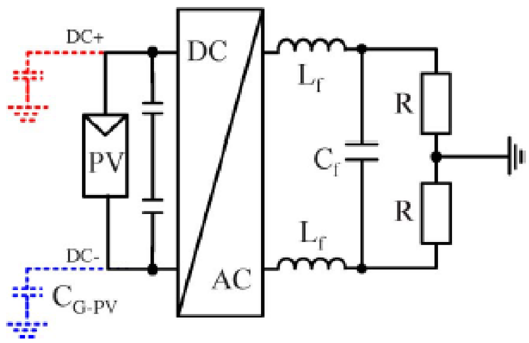

Figure 2. *Test setup used for common-mode voltage measurement.*

In the following, simulation results obtained using MATLAB/SIMULINK are shown. The simulation step size is 0.1 μs, with an 8-kHz switching frequency.

Simulation parameters:

Lf = 1.8 mH filter inductance;

Cf = 2 μF filter capacitance;

R = 7.5 Ω load resistance;

Vdc = 350 V input dc voltage;

Cdc = 250 μF dc-link capacitance;

*C*G−PV = 100 nF parasitic capacitance of PV array;

*F*sw = 8 kHz switching frequency for all cases except that the switching frequency for unipolar

Pulse width modulation (PWM) has been chosen to be *F*sw = 4 kHz, so the output voltage of the inverter has the same frequency for all cases.

2.1 HB-ZVR Topology

Another solution for generating the zero-voltage state can be done using a bidirectional switch made of one IGBT and one Diode Bridge. The topology is detailed in Fig. 3, showing the bidirectional switch as an auxiliary component with a gray background. This bidirectional switch is clamped to the midpoint of the dc-link capacitors in order to fix the potential of the PV array also during the zero-voltage vector when S1–S4 and S2–S3 are open. An extra diode is used to protect from short-circuiting the lower dc-link capacitor.

During the positive half-wave, S1 and S4 are used to generate the active state, supplying a positive voltage to the load, as shown in Fig. 3. The zero-voltage state is achieved by turning on S5 when S1 and S4 are turned off, as shown in Fig. 4. The gate signal for S5 will be the complementary gate signal of S1 and S4, with a small dead time to avoid short-circuiting the input capacitor. By using S5, it is possible for the grid current to flow in both directions; this way, the inverter can also feed reactive power to the grid, if necessary.

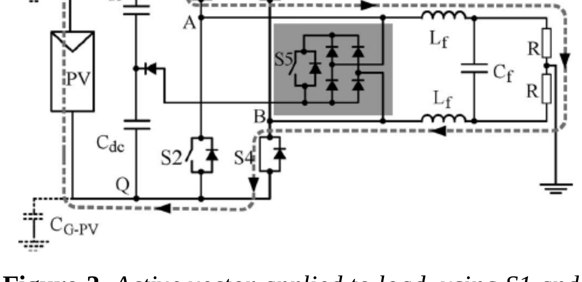

Figure 3. *Active vector applied to load, using S1 and S4 during positive half-wave.*

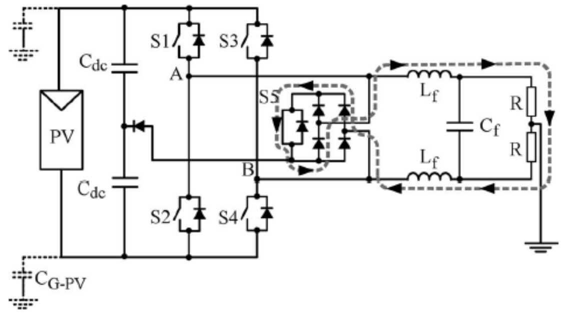

Figure 4. *Zero vectors applied to load, using S5 during positive half-wave.*

During the negative half-wave of the load voltage, S2 and S3 are used to generate the active vector and S5 is controlled using the complementary signal of S2 and S3 and generates the zero voltage state, by short-circuiting the outputs of the inverter and clamping them to the midpoint of the dc-link.

During the dead time, between the active state and the zero state, there is a short period when the freewheeling current finds its path through the anti parallel diodes to the input capacitor while all the switches are turned off. This is shown in Fig. 5 and leads to higher losses, compared to the HERIC topology, where the freewheeling current finds its path through the bidirectional switch, either through S5 or S6, depending on the sign of the current.

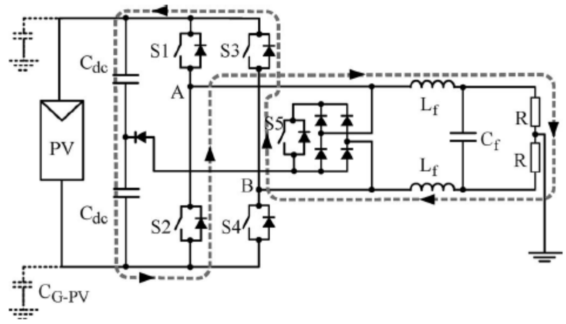

Figure 5. *Dead time between turnoff of S1 and S4 and turn on of S5 during positive half-wave.*

As shown in Fig. 6, the output voltage of the inverter has three levels, taking into account the freewheeling part during dead time. In this case the frequency is equal to the switching frequency.

To show that this topology does not generate a varying common-mode voltage, V_{cm} has been calculated for the switching states regarding the positive, zero, and negative vectors

$$V_{cm} = \frac{V_{AQ}+V_{BQ}}{2} \quad (1)$$

$$V_{AQ} = V_{dc}; V_{BQ} = 0 \Rightarrow V_{cm} = \frac{V_{dc}}{2} \quad (2)$$

$$V_{AQ} = \frac{V_{dc}}{2}; V_{BQ} = \frac{V_{dc}}{2} \Rightarrow V_{cm} = \frac{V_{dc}}{2} \quad (3)$$

$$V_{AQ} = 0; V_{BQ} = V_{dc} \Rightarrow V_{cm} = \frac{V_{dc}}{2} \quad (4)$$

As detailed by (1)–(4), the common-mode voltage is constant for all switching states of the converter. Therefore, the leakage current through the parasitic capacitance of the PV as shown in Fig. 7.

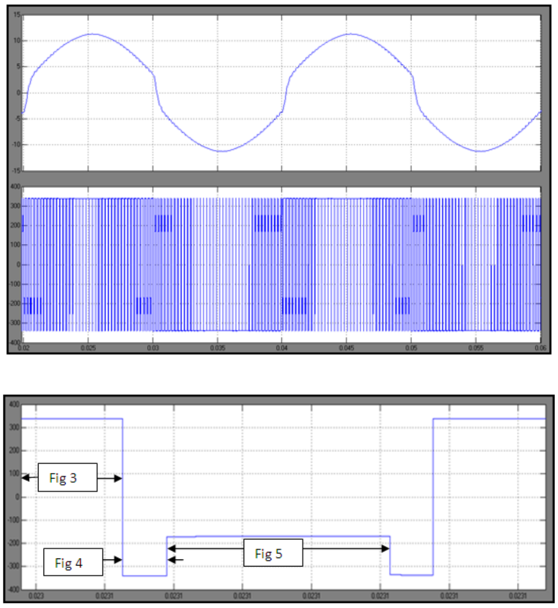

Figure 6. *HB-ZVR load current and inverter output voltage.*

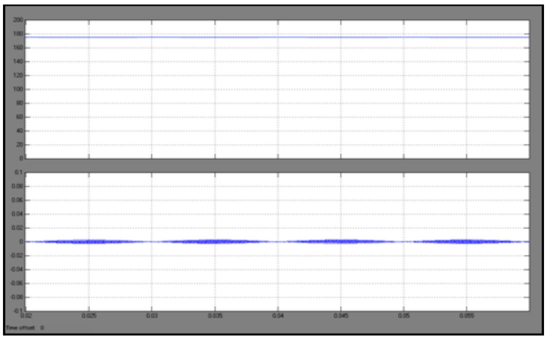

Figure 7. *HB-ZVR Voltage to ground and ground leakage current.*

2.2 Proposed Topology (NPCMLI)

The diode clamp method can be applied to higher level converters. As the number of level increases, the synthesized output waveform adds more steps, producing a staircase waveform. A zero harmonic distortion of the output wave can be obtained by an infinite number of levels.

In this paper, a single-phase diode clamped multilevel inverter or Nutral point clamped multi level inverter is used to reduce the ripple at load side inorder to provide pure sine waveform.

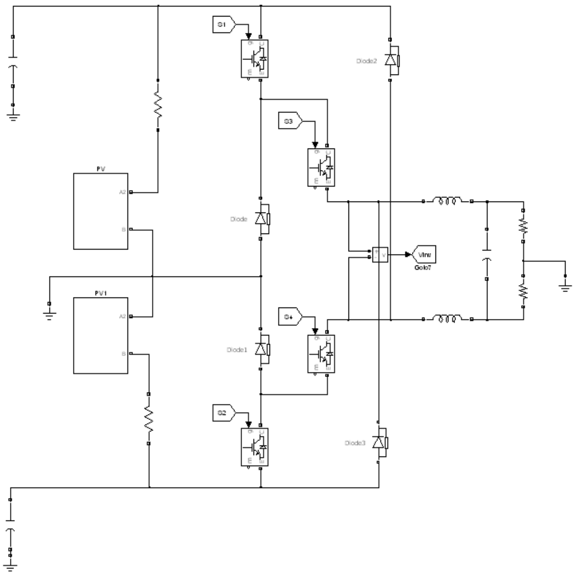

Figure 8. *NPC multilevel inverter connected PV-Grid system*

The nutral point clamped grid conncted pv inverter structure is as shown in th fig.8 which gives the less total harmonic distortion compared to the conventional topologies.

As shown in Fig. 9, the output voltage of the inverter has three levels, taking into account the freewheeling part during dead time. In this case also, the load current ripple is very small. Therefore, the leakage current through the parasitic capacitance of the PV would be very small, as shown in Fig. 10.

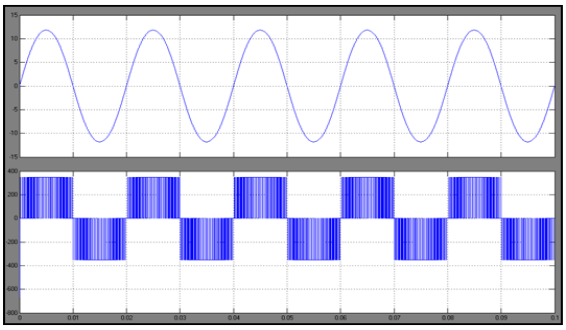

Figure 9. *Load current and inverter output voltage by NPCMLI*

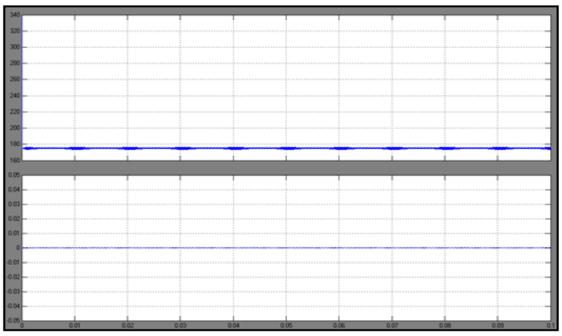

Figure 10. *Voltage to ground and ground leakage current by NPCMLI*

3. CONCLUSION

Transformer less inverters offers a better efficiency, compared to those inverters that have a galvanic isolation. On the other hand, in case the transformer is omitted, the generated common-mode behavior of the inverter topology greatly influences the ground leakage current through the parasitic capacitance of the PV.

Bipolar PWM generates a constant common-mode voltage, but the efficiency of the converter is low, due to the two level output voltage. By using unipolar PWM modulation, the output of the converter will have three levels, but in this case, the generated common-mode voltage will have high-frequency components, which will lead to very high ground leakage currents.

This paper has introduced a transformer less topology and given an alternative solution for the bidirectional switch, used to generate the zero-voltage state. A NPCMLI is used to provide reduced harmonic voltage to the grid to reduce the harmonics at load current.

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