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Design Implementation of 32-bit Twin Precision Low Power Re-Configurable Multiplier

P Surya

PG Scholar, Department of ECE, Aurora's Technological and Research Institute,
JNTUH, Telangana, India
surya.padma@yahoo.in

K Srinivas

Assistant Professor, Department of ECE, Aurora's Technological and Research Institute,
JNTUH, Telangana, India
Kotha.srinivas.428@gmail.com

Abstract: *In a signal processing like application, the performance of the whole processing is a function of how fast the FFT operation is done .The speed of the operation is directly dependent on efficiency of the multiplier in the design. The paper discusses about a multiplier implementation where the speed of computation is improved by using twin-precision scheme and row decomposition schemes. To lower the dynamic power consumption we have involved the concept of clock gating .The proposed architecture permits the optimization of the speed and power. The design is a purely combinational logic based circuitry internally, involving a clock for data reliability. A comparison between 32 bit and 16-bit multipliers, one working on twin precision scheme compared to regular HPM, shows that the twin-precision multiplier has significant lower power dissipation and 35% higher speed with a trade off in more transistors. The implementation of the design is carried at 32nm and 90nm using Synopsys VCS, DC and ICC.*

Keywords: *High-Speed, Clock gating, Multipliers, Re-configurable, Twin-precision, Excess-1-Adder, Row decomposition.*

1. INTRODUCTION

Any m-bit by n-bit multiplication has a possibility to have a maximum output that is m+n bit wide, the difference in the bit width is one of the reasons for excessive power dissipation and long delays Multiplication is a complex arithmetic. The operation has a large circuitry involved so will be its signal propagation delay and power dissipation. The desire for increased functionality using the same circuitry and an associated capability to adapt to changing requirements has led to the design of re-configurable architectures. Increased area, complex routing and static power dissipation are the major problems that are to be faced when reconfigurability is opted.

To improve the speed of multiplication, we have involved the concept of row decomposition that has the ability to solve the partial product array very quickly when compared to the conventional methods. The N X N multiplier design involves whole four N/2 X N/2 multipliers and they are routed along with additional logic to produce a final product that is 2N bits wide. The concepts involved in twin-precision is explained in section II, the architecture of multipliers are discussed in section III, the row decomposition techniques for partial products are discussed in section IV. The simulation, synthesis and post routing results are given in section V.

2. TWIN PRECISION FUNDAMENTALS

In an unsigned binary multiplication each bit of one of the operands, called the multiplier, is multiplied with the second operand, called multiplicand. That way one row of partial products is generated. Each row of partial products is shifted according to the position of the bit of the multiplier, forming the partial-product array. Finally, partial products that are in the same column are summed together, forming the final result

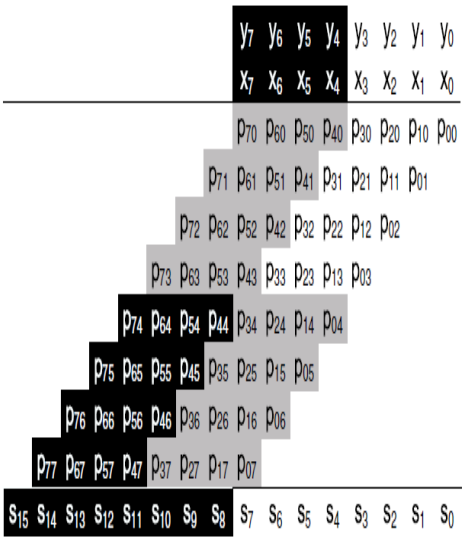

Fig 1. *Illustration of an unsigned 8-bit multiplication, where a 4-bit multiplication, shown in white, is computed in parallel with a second 4-bit multiplication, shown in black.*

If, there is a way of setting unwanted partial products to zero, then it becomes possible to partition the multiplier into two smaller multipliers that can compute multiplications in parallel. In the above illustrations the two smaller multiplications have been chosen such that they are of equal size. This is not necessary for the technique to work.

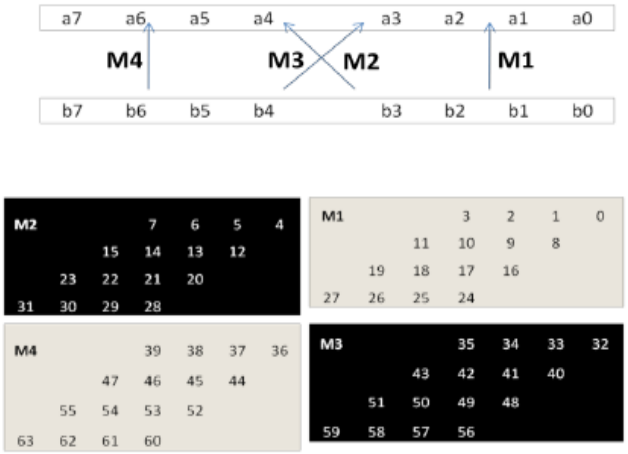

Fig 2. *Illustration of an unsigned 8-bit multiplication as four sub multiplications involved.*

Any size of the two smaller multiplications can be chosen, as long as the precision of the two smaller multiplications together are equal or smaller than the full precision (NFULL) of the multiplication are two smaller multiplications, they are referred to as the multiplication in the Least Significant Part (LSP) of the partial-product array with size NLSP, shown in white, and the multiplication in the Most Significant Part (MSP) with size NMSP , shown in black.

In twin precision multiplier it is possible to perform two N/2-bit multiplications in parallel in an N-bit multiplier. One N/2 × N/2–bit multiplication is performed using N/2 × N/2-bit partial product bits in the least significant part of the multiplier and another N/2 × N/2-bit multiplication using partial product bits in the most significant part. The resulting products are the least significant and most significant halves of the output, respectively. Design is such that we can configure multiplier according the application needed.

3. THE ARCHITECTURE OF MULTIPLIER

Consider the multiplier and multiplicand in NLSP NMSP, main multiplier can be considered to have four multiplier blocks as shown in the figure 3

3.1 N/2 X N/2 Multiplier Block

The architecture of recursive multiplier for N x N bit multiplier with RCA as merging adder has four multipliers Each N/2 multiplier in uses HPM algorithm .In order to form the original 2N bit product the inter dependency of the multipliers must be satisfied.

This phase covers till partial product array compression in figure 3

3.2 Clock Gating

Integrated clock gating(ICG) is employed in the design .In the design clock gating is used for achieving operator isolation in the Recursive multiplier for power reduction. As mentioned earlier recursive multiplier has four N/2 bit multipliers of which M2 and M3 are dependent and M1 and M4 are independent. So to achieve low power and double-throughput are using clock gating technique and are isolating the M2 and M3 multipliers without transferring inputs them. To perform twin precision multiplication an extra control input is needed. Here are considering a two it input "Twin" as a control input. The "Twin" is passed through a 2:3 decoder which generates T[1], T[2] and T[3] as control signals and these signals are used for the operator isolation.

Clock gating saves power by adding more logic, to circuit to conditionally enable the clock tree. Control on the clock helps us disable portions of the circuitry so that the basic blocks linked in them do not have to switch states.

Switching states consumes power. When not being switched, the switching power consumption goes to zero, and only leakage currents are incurred.

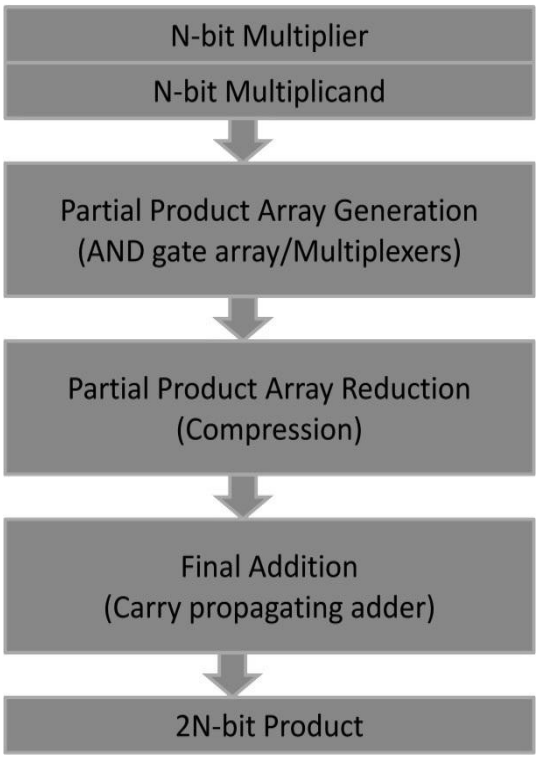

Fig 3. *Block diagram specifying the steps involved in N X N multiplier design as*

3.3 Ripple Carry Adder and Multiplexer Block

The partial products of M2 and M3 multipliers over lap. So we design the addition with a ripple carry adder. The output is N+1 bits wide. Similar data dependencies can be observed from the figure 4

If there exists a carry propagated by the N+1 bit RCA, it is to be forwarded to the M4 multiplier's MSB. The carry signal serves as a selection line whether to add 1 to the MSB. This is interpreted to serve as a multiplexer with carry line as selection pin, inputs being the MSB portion left.

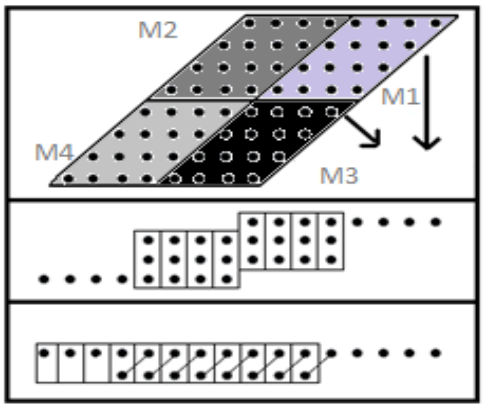

Fig 4. *Illustration of an unsigned 8-bit multiplication and the data dependencies present in the outputs of the sub multipliers.*

For carry to be propagated to MSB Instead of using RCA , the implementation has been done by Excess -one converter is used that consumes much lower hardware and and also offers faster computational flex

3.4 Reordering of Partial Product

The partial product array is formed completely by using 'AND' gates Reordering of partial product involves three important phases

Phase 1 The partial products are formed as parallelogram structure.

Stage 2 The parallelogram structure of partial products is rearranged

Stage 3 Finally, the reordering of partial products is done by moving all the IMP partial products to the higher height of the partial product tree. ibility

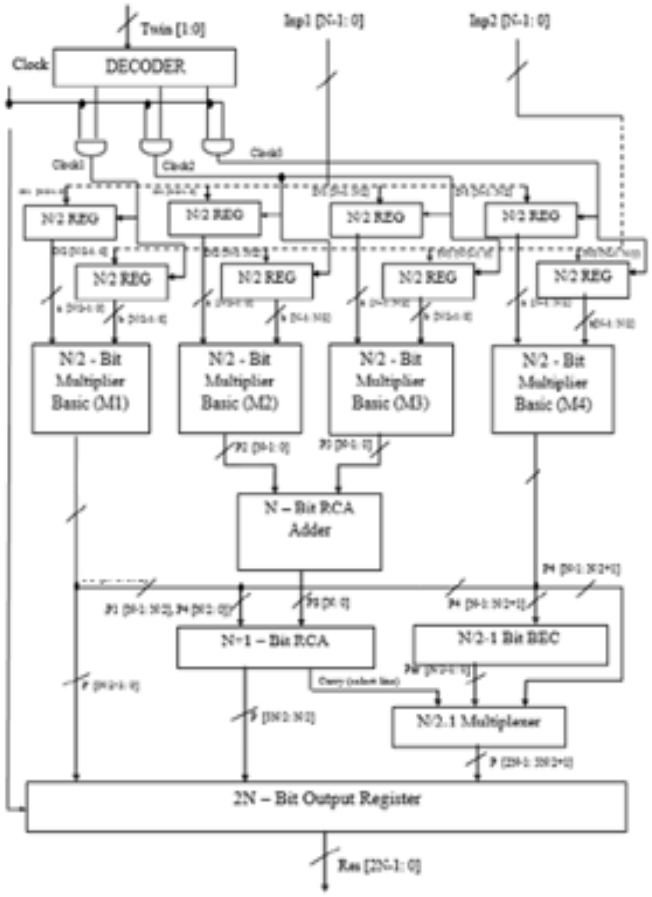

Fig 5. *Architecture of the multiplier designed*

3.5 Row Decomposition Fundamentals

The column compression is done using High Performance Multiplier. In the HPM algorithm, the height of the tree is reduced by one for each row. For example rows 8, 7, 6, 5, 4, 3, 2 for an 8-bit multiplier. By using this column compression technique the height of the tree is reduced to two. The final addition is performed by using ripple carry adder. Apart from HPM scheme there are other approaches like Dadda Algorithm, Wallace Tree based row decomposition. They comparatively are considered to have a complex routing when compared to HPM[1]

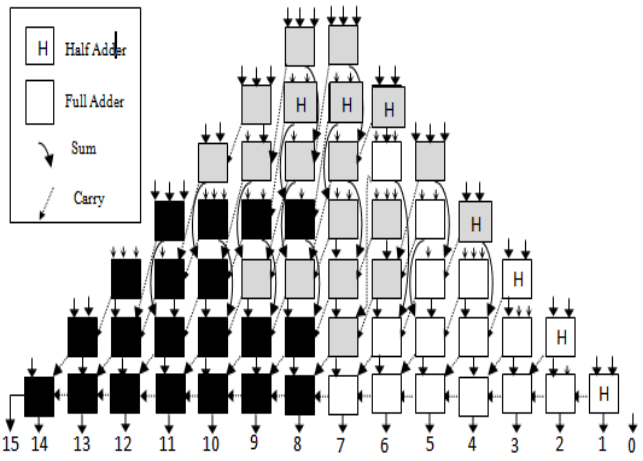

Fig6. *Architecture of an unsigned 8-bit twin precision multiplier by using reordering of partial products and HPM reduction tree*

The advantage in using HPM is preferable due to the regularity in the routing. The block diagram for unsigned 8-bit twin precision multiplier by using reordering of partial products and HPM reduction tree is shown in the figure 6. The proposed architecture showed that the transition that are taking place in carrying out N X N multiplication and N/2 X N/2 mode is reduced compared to basic HPM resulted in reduce switching power.

At 32nm technology node the 16 X 16 HPM multiplications is compared with 16 X 16 twin precision multiplier that uses four 8 X 8 multipliers. The power analysis showed 52 % lower consumption in the case of twin precision approach.

Table I. *The Hardware Involved in N X N HPM Multiplier Design*

Multiplier	No. of FAs	No. of Has	CPA Length
HPM	N^2-4N+3	N-1	2.N-2

4. IMPLEMENTATION RESULTS

8 bit HPM

16 bit HPM

32 bit HPM

16 bit Twin Precision

32 bit Twin Precision

16 bit re-configurable Twin Precision multiplier

32 bit re-configurable Twin Precision multiplier

Are implemented using the schemes mentioned in the sections above. The designs are coded using Verilog HDL, Simulation is done in Synopsys VCS. Synthesis is performed using Synopsys Design Compiler at 32nm and 90nm technology nodes. The timing and power reports show that it has less power consumption in single precision mode, but it has higher power consumption in full precision. The clock gated design showed a significant fall in the dynamic power. The timing and power characteristics are drawn and tabulated in Table II. Comparing the power repots in 32nm technology node with 90nm technology node there is a drastic increase in the leakage power observed. Figures 7, 8, 9 and 10 show the graphical representation of power reports and timing reports

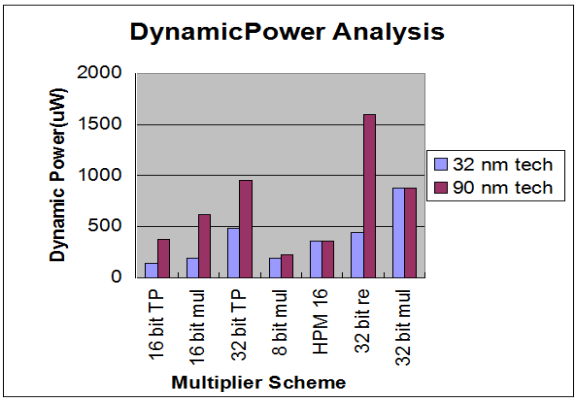

Fig 7. *Graph showing dynamic power in 32nm and 90nm for various implementations*

The physical design flow is carried out for every design and the GDSII format file is created.

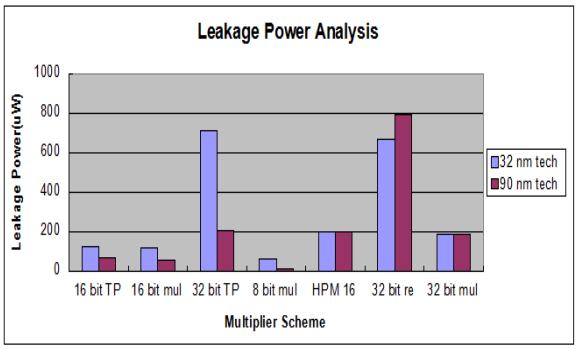

Fig 8. *Graph showing leakage power in 32nm and 90nm for various implementations*

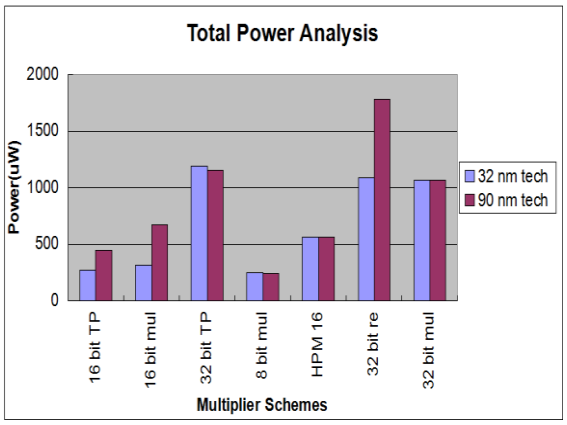

Fig 9. *Graph showing power in 32nm and 90nm for various implementations*

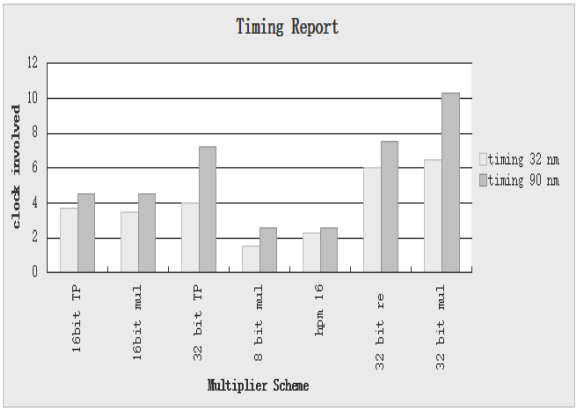

Fig 10. *Graph showing timing variations in 32nm and 90nm for implementations*

Above graphs are taken from 32nm and 90nm synthesis reports , when constrained to typical library setup. The speed improved in the design for 32 bit twin precision multiplier and the 32 HPM multiplier is 35%.

Table 2. *The results drawn from the implementations at 90nm*

Multiplier	32nm synthesis reports		
	Area(um^2)	Power(uW)	Timing(ns)
32 bit TP re	11149.92	1195.10	4.0
32 bit recursive	9874.81	1091.02	6.0
HPM 32	12374.13	1175.03	6.5
16 bit recursive	3203.07	275.81	3.7
16 bit multiplier	2999.26	316.84	3.5
HPM 16	2815.44	562.03	2.3
Bit 8 multiplier	768.70	252.91	1.5

TABLE 3. *The Results Drawn From Various Implementations At 32nm*

Multiplier	90nm synthesis reports		
	Area(um^2)	Power(uW)	Timing(ns)
32 bit TP	49395.33	1158.9	7.2
32 bit recursive	46818.34	1783.03	7.5
HPM 32	49467.98	1066.12	10.3
16 bit TP	15378.24	447.36	4.5
16 bit recursive	13208.07	674.09	4.5
HPM 16	12011.38	654.03	2.6
Bit 8 multiplier	3826.24	240.62	2.6

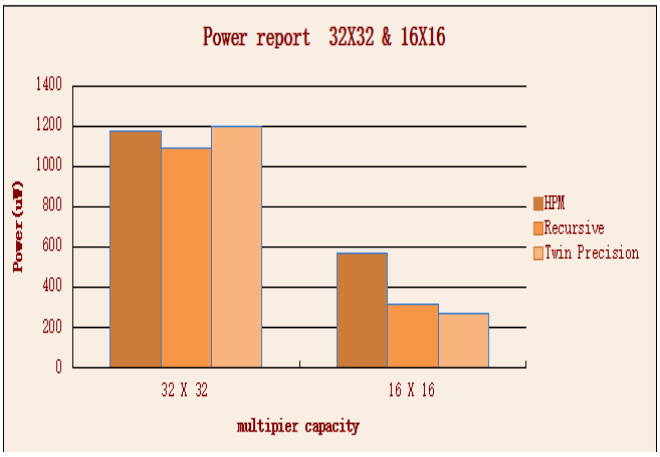

Fig 11. *Graph showing dynamic power in 32nm for HPM ,Recursive and Twin Precision*

5. CONCLUSIONS

In this paper, reordering of partial products technique for HPM based unsigned multiplication is designed. The results show that there is a drastic change in the dynamic power due to clock gating.

The leakage power in lower technology has a very prominent. The power consumption is optimized using HPM and twin precision .We have observed that power cut-off techniques can be deployed in different regions of a twin-precision functional unit, so that static leakage reduction can be effected not only when the entire unit is idle, but also when only parts of the unit are active, i.e. when the unit operates in half-precision mode.

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