

Reduced Area Carry Select Adder with Low Power Consumptions

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ABSTRACT

In many computers and other kinds of processors the adder is the most commonly used arithmetic block. In this paper, we proposed an area-efficient carry select adder that also having low power consumptions. In this, by sharing the common Boolean logic term, we can reduce the duplicated adder cells that used in the conventional carry select adder. So we only need one XOR gate and one inverter gate for each summation operation as well as one AND gate and one OR gate in each carry-out operation. The multiplexers used to select the correct output result according to the logic state of carry-in signal. The proposed 64 bit carry select adder, simulated for 180nm CMOS technologies, has reduced transistor count as well as power delay product reduced than that of conventional carry select adder.

Keywords: Carry select adder, area efficient, low power

INTRODUCTION

In many computers, Digital Signal Processors and other kinds of processors the adder is the most commonly used arithmetic block. Adder is used in the arithmetic logic units, and also in other parts of the processor, where it is used to calculate addresses, table indices, and similar operations. As the adder is mostly used in the Central Processing Unit (CPU) and Digital Signal Processing (DSP), therefore its performance parameters and power optimization is of utmost importance [3]. Due to the increasing popularity of portable electronic devices the size of the technology is shrinking. At the same time, the power consumption per chip also increases significantly due to the increasing density of the chip. Therefore, in realizing modern Very Large Scale Integration (VLSI) circuits, low-power and high-speed are the predominant factors which need to be considered. Like other circuits' design, the design of high-performance and low-power adders can be addressed at different levels, such as architecture, logic style, layout, and the process technology. As the result, there is always existing a trade-off between the design parameters such as speed, power consumption, and area [5]. Our objective is to design a lower-power and smaller area as a prime consideration. The ripple carry adder is simple design, but it is the slowest types of adders, carry propagation delay (CPD) is main concern in this [12]. To improve the shortcoming of carry ripple adder to remove the linear dependency between computation delay time, carry select adder is presented [5].

CONVENTIONAL CARRY SELECT ADDER

Carry select adder comes in the types of conditional sum adders. Conditional sum adders work on some conditions [3]. A carry-select adder generally consists of two ripple carry adders (RCA) and a multiplexer. Addition of two n-bit numbers with a carry-select adder is done with two ripple carry adders that perform the calculation twice, one time with the assumption of the carry being zero and the other assuming one. When these two results are calculated, the correct sum, and the correct carry, is selected with the multiplexer once the correct carry is known.

The carry select adder divides the ripple carry adder into M parts, while each part consists of a duplicated (N/M)-bit two carry ripple adders. From these two carry ripple adders, one is calculated as carry input value is logic "0" and another ripple carry adder is calculated as carry input value is logic

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“1”. When the actual carry input is ready, either the result of carry input value “0” path or the result of carry value “1” path is selected by the multiplexer according to its correct carry input value [5]. The figure 1 shows 16-bit carry select adder is divided the carry ripple adder into 4 parts, while each part consists of a duplicated 4-bit carry ripple adder pair.

An n-bit Carry select adder consists of ‘n’ full adders with the carry signal that ripples from one full-adder stage to the next, i.e. from LSB to MSB. It is possible to create a logical circuit using several full adders to add multiple-bit numbers. A C_{in} is the carry input for each full adder which is the C_{out} of the previous adder. Addition of k-bit numbers can be completed in k clock cycles.

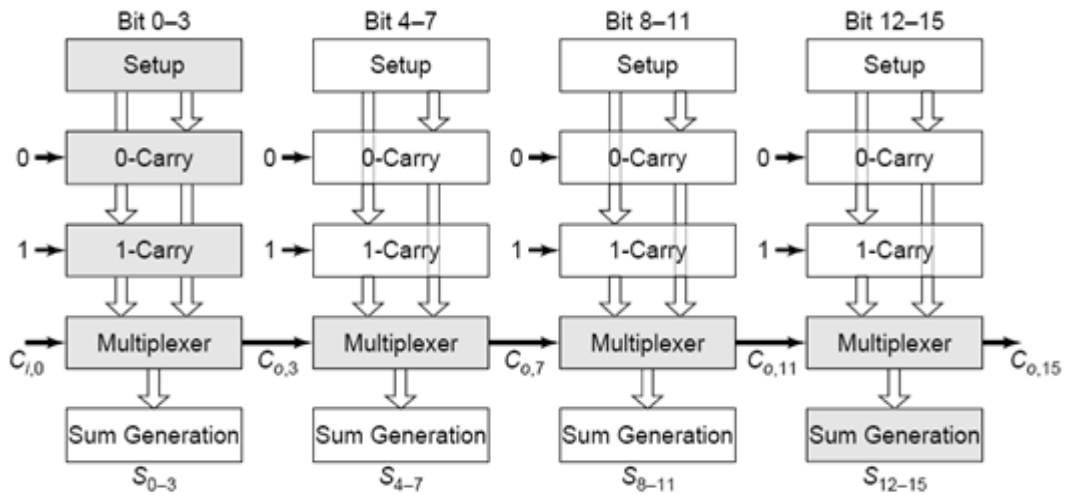


Fig1. The 16-bit carry select adder is divided the carry ripple adder into 4 parts, while each part consists of a duplicated 4-bit carry ripple adder pair.

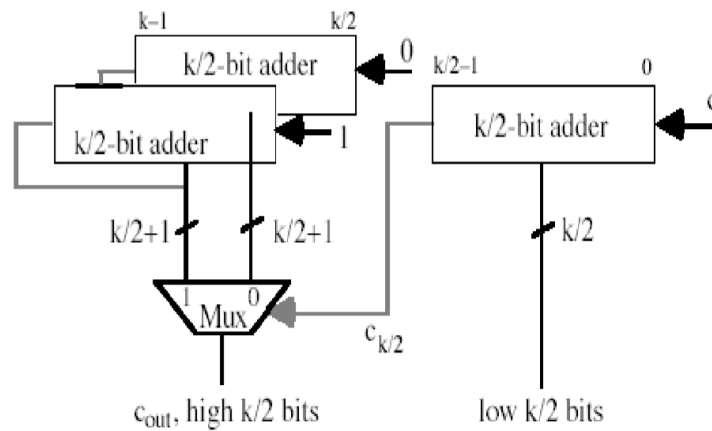


Fig2. Block diagram of k-bit adder

CARRY SELECT ADDER WITH BEC

The Binary to Excess one Converter (BEC) replaces the ripple carry adder (RCA) with $C_{in}=1$. The main idea of this work is to use BEC instead of the RCA with $C_{in}=1$ in order to reduce the area and power consumption of the regular CSLA [7]. BEC uses less number of logic gates than N-bit full adder structure. To replace the n-bit RCA, an n+1 bit BEC is required [11]. BEC is a circuit used to add 1 to the input numbers as shown in Fig. 3. Boolean expressions of 4-bit BEC are listed below (Note: symbols ~NOT, &AND and ^XOR)

$$X0 = \sim B0$$

$$X1 = B0 \wedge B1$$

$$X2 = B2 \wedge (B0 \wedge B1)$$

$$X3 = B3 \wedge (B0 \wedge B1 \wedge B2)$$

Therefore, CSA using BEC has low power and less area than conventional CSA. Sqrt CSLA has been chosen for comparison with modified design using BEC as it has more balanced delay, less area and low power. The figure-4 shows block diagram for CSA using BEC. One input to the mux goes from the RCA with $C_{in}=0$ and other input from the BEC. Comparing the group 2 of both regular and modified CSLA, it is clear that BEC structure reduces the area and power [8].

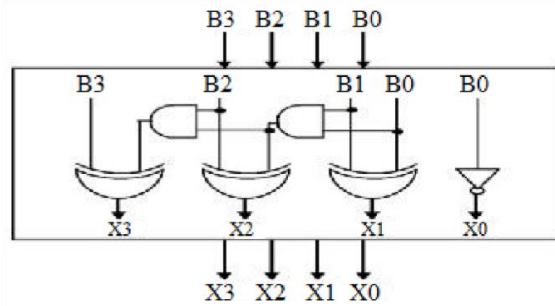


Fig3. 4-bit binary to excess one converter

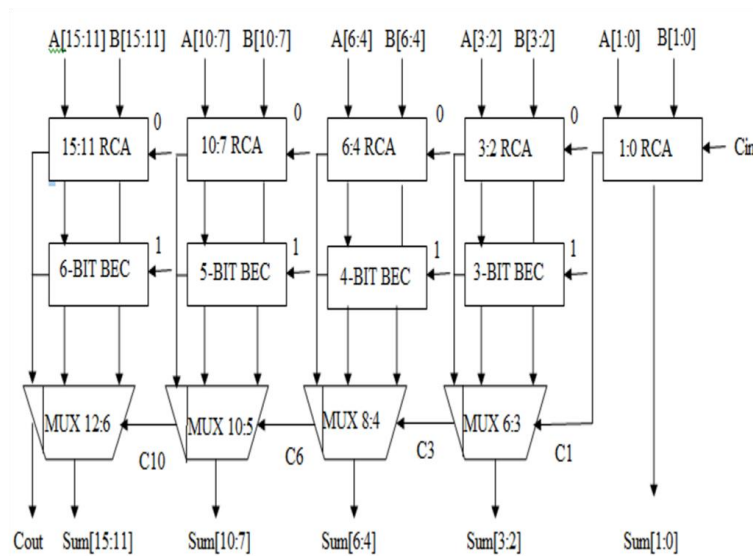


Fig4. Carry select adder using BEC

AREA-EFFICIENT CSA USING COMMON BOOLEAN LOGIC

To remove the duplicate adder cells in the conventional CSLA, an area efficient Sqrt CSLA is proposed by sharing Common Boolean Logic (CBL) term [11]. Through analysing the truth table of a single-bit full-adder, we can find out that the output of summation signal as carry-in signal is logic “0” is the inverse signal of itself as carry-in signal is logic “1”. S_0 is “0110” as C_{in} is logic “0” and S_0 is “1001” as C_{in} is logic “1” [5].

Table1. The truth table of one-bit full adder, where the upper part is case of $C_{in}=0$ and lower part is the case of $C_{in}=1$.

C_{in}	A	B	S_0	C_0
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

To share the common Boolean logic term, we only need to implement one XOR gate and one INV gate to generate the summation signal pair. As actual carry-in signal is ready, we can select the correct summation output signal according to the logic state of carry-in signal. As for the carry propagation path, we need one OR gate and one AND gate to count possible carry input values in advance. Once the carry-in signal is ready, we can select the correct carry-out output according to the logic state of input carry signal. The figure 5 shows area-efficient carry select adder with common Boolean logic sharing.

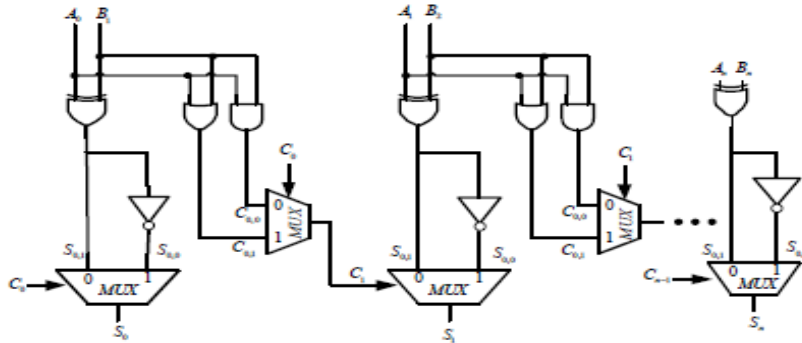


Fig5. Internal structure of the proposed area-efficient carry select adder is constructed by sharing the common Boolean logic term

TANNER TOOL SIMULATION RESULTS

The work has been developed using Tanner Tool version 7. This architecture proposed for 32 bit and 64-bit carry select adder. The figure 6 shows the schematic diagram for one-bit carry select adder using tanner tool.

The transistor count of our area-efficient carry select adder could be reduced to be very close to that of carry ripple adder, the transistor count in the conventional carry select adder is nearly double as compared with the proposed design.

The area-efficient carry select adder achieve an outstanding performance in power consumption. Power consumption can be greatly saved in area-efficient carry select adder because we only need one XOR gate and one INV gate in each summation operation as well as one AND gate and one OR gate in each carry-out operation after logic simplification and sharing partial circuit. We simulated the power consumption in the proposed area-efficient adder and the conventional carry select adder with 32-bit and 64-bit in 0.09 μ m 0.18 μ m CMOS technology. The table 2 shows the comparative results analysis for the conventional carry select adder and proposed area-efficient carry select adder. The compared results show that the area efficient carry select adder has lees delay, reduced area, lower power consumptions and less power delay product. The figure 7 shows relative output waveforms result for area-efficient carry select adder.

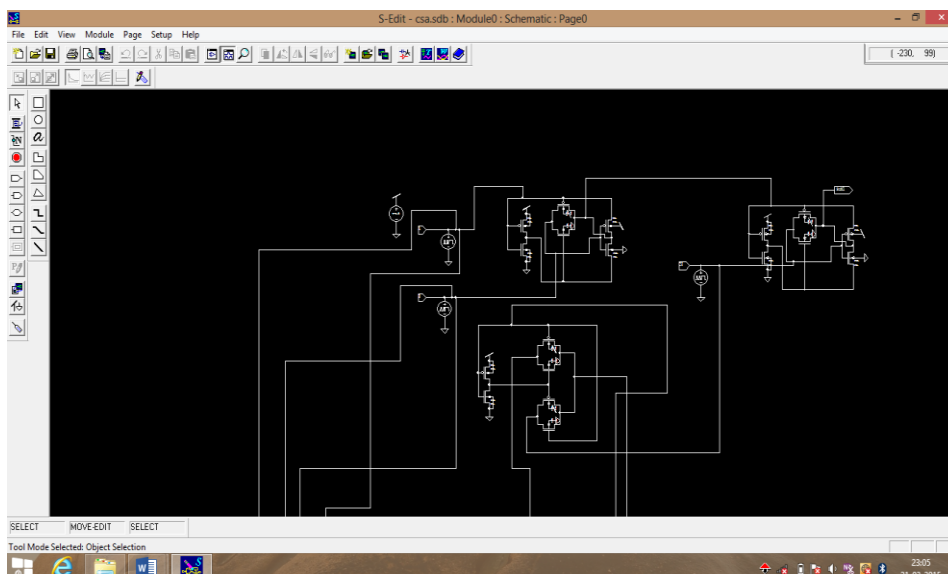


Fig6. schematic diagram for one bit CSA using tanner tool version 7

Table2. Simulation results for area, power and delay.

Design style	Technology file (μm)	Avg. power consumptions(watts)	Prop. delay at sum (sec)	Power delay Product (pws)
Conventional CSA	0.09	95.49×10^{-3}	5.19×10^{-10}	4958.222
Area-efficient CSA	0.18	5.71×10^{-3}	1.62×10^{-10}	92.502
Area-efficient CSA	0.09	4.96×10^{-3}	1.41×10^{-10}	69.936

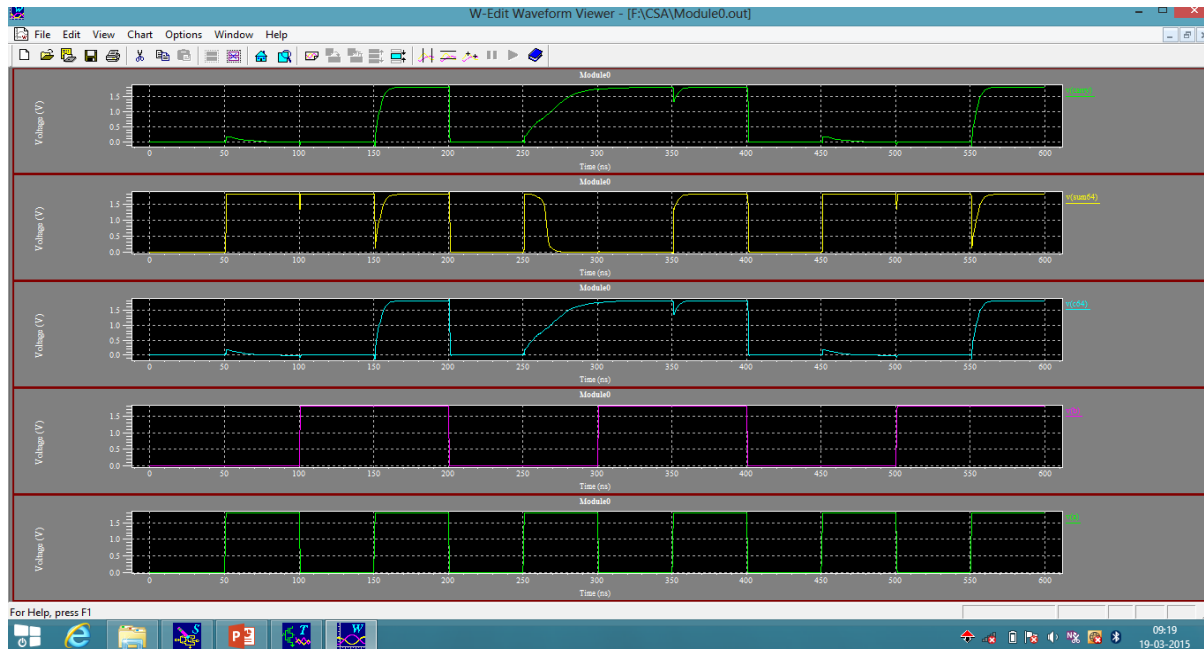


Fig7. Simulated waveforms results for sum and carry-out outputs of carry select adder.

CONCLUSION

In this paper, an area-efficient carry select adder (CSA) is proposed. By sharing the common Boolean logic term, we can remove the duplicated adder cells in the conventional carry select adder. This work presents a simple approach to reduce the area, delay and power of CSLA architecture. The proposed 64 bit carry select adder, simulated for 180nm CMOS technologies using Tanner Tool version 7, and gives much better results than that of conventional carry select adder. The proposed area efficient carry select has lesser transistor count and reduced power delay product which makes it efficient for VLSI hardware implementations.

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