International Journal of Emerging Engineering Research and Technology
Volume 3, Issue 7, July 2015, PP 147-151
ISSN 2349-4395 (Print) & ISSN 2349-4409 (Online)

Implementation and Analysis of High Speed and Area Efficient Carry Select Adder

Madhurima Bose[1], Sourabh Sharma[2]

[1]*PG Scholar, Trinity Institute of Technology & Research, Bhopal*
[2]*Assistant Professor, Trinity Institute of Technology & Research, Bhopal*

ABSTRACT

In today's scenario of VLSI system designing, efficient area designing, low power and high speed processing is developing as large research area. Every programmer has to think about these parameters to design a systematic highly efficient program, which satisfies certain conditions. That condition which satisfactorily overcome the large area problem, high power consumption and relatively work on delay of the circuit. As there are many adder circuits, here we are going to modify the Carry Select Adder (CSLA) using logical converter unit (LCU) which similarly works as Binary to Excess -1 convertor (BEC), but changes is done in the gate level modelling, due to which it reduces size or area, delays are more less and low power is required. The proposed work is implemented on 8-bit, 16-bit, 32-bit and 64-bit. The study also shows the comparison between Regular Carry Select Adder (RCSLA) and redesigned the Carry Select Adder using Logical Converter Unit (LCU) having reduced area and delay. This proposed work uses a simple and efficient gate-level modification to significantly reduce the area and power of the 64 bit Carry Select Adder (CSLA) .The proposed design has reduced area and power which is implemented in Verilog design in Xilinx ISE 8.2i.

Keywords: CSLA, RCA, Binary to Excess-1, Logical Converter Unit

INTRODUCTION

In the VLSI system design, the main areas of research are the reduced size & high speed path logic systems. A fundamental requirement of high speed addition and multiplication is always needed for the high performance processors. In the digital system, the speed of addition depend on the propagation of carry which is generated sequentially after the previous bit has been summed & carry is propagated into the next position. There are many types of adders available such as Ripple Carry Adder, Carry Look Ahead Adder, Carry Save Adder, Carry Skip Adder and Carry Select Adder, which have their own advantages & disadvantages.

The major limitation of speed in any adder is in the production or generation of carries and its propagation, due to which delay occurs in the computation process and dealing with this we have to consider other parameters also such as area and power consumption. Many authors considered this as important problem and try to implement an efficient adder circuit.

As there are many adder circuits, here we are going to modify the Carry Select Adder (CSLA) using logical converter unit (LCU) which similarly works as Binary to Excess -1 convertor (BEC), but changes is done in the gate level modelling, due to which it reduces size or area, delays are more less and low power is required. The proposed work is implemented on 8-bit, 16-bit, 32-bit and 64-bit. The study also shows the comparison between Regular Carry Select Adder (RCSLA) and redesigned the Carry Select Adder using Logical Converter Unit (LCU) having reduced area and delay.

This proposed work uses a simple and efficient gate-level modification to significantly reduce the area and power of the 64 bit Carry Select Adder (CSLA) .The proposed design has reduced area and power which is implemented in Verilog design in Xilinx ISE 8.2i. The proposed work on the Carry Select Adder also shows that if we increasing word size, we can design variable or uniform pattern of the bits in such a way, which reduces the size of adder and provides relatively less delay and low power consumption.

Address for correspondence:

madhurimab.bose@gmail.com

This paper is having different sections which are as follows: Section II, literature survey of the circuit which shows how to evaluate area and delay of basic gates are done. Section III, shows the Binary to Excess1 Converter, Section IV, explains about conventional Carry Select Adder using RCA and also evaluates their area and delay. Section V shows the proposed method of using Logical Converter Unit (LCU) and how its impact in the area and delay of the adder circuit and Section VI, shows the simulation results and conclusion.

LITERATURE SURVEY

Rajkumar and Kittur[4], shows an efficient gate level modification to significantly reduce the area and power of the Carry Select Adder (CSLA). On this modification author compare 8bit, 16 bit, 32 bit, and 64 bit regular SQRT Carry Select Adder with modified Carry Select Adder (CSLA) and got the result in the form of less area and reduced power. In the modified architecture author uses Binary to Excess-1 convertor with carry 1 in place of Ripple Carry Adder (RCA) which is used in the regular SQRT Carry Select Adder circuit. Samiappa Sakthikumaran [3], [5], [6] with others proposed a basic unit, in which gate level modification is done and Boolean expression were made. The basic gate level circuit is easily implemented and delay will be easily evaluated with simple expressions it become easily understandable. P.Ramani proposes an efficient method which replaces Ripple Carry Select Adder using Binary to Excess-1 convertor and provide us low power 256 bit Modified Carry Select Adder (CSLA). This proposed work shows its impact in delay as well comparing with regular SQRT Carry Select Adder (CSLA) [1].

Evaluation of Area and Delay of Logical Gates

Evaluation of the area and delay of the adder circuit is based on the basic gates, i.e. implementation of XOR gate by using AND gate, OR gate and Inverter [4] as shown in the fig. 1. For the evaluation of delay, we assumed that one gate introduces delay of 1ns, so that if the circuit consist of only one gate then delay count will be 1ns (i.e. one AND gate = 1ns). Therefore, if there are three basic logic gates, it will produce delay of 3ns, but is this evaluation delay produce by the Inverter is negligible. Therefore, for designing of XOR gate, we require two Inverters, two AND gates and one OR gate show delay of 3ns (i.e. AND gate = 2ns + OR gate = 1ns). Taking these considerations the delay of the overall circuit is evaluated. When the area count is done, each and every logical gate occupies the space, they are represent as one unit (i.e one Inverter = 1unit), therefore when area of XOR gate is counted, it is given by 5 (2 Inverter + 2 AND + 1OR = 5 units). Similarly, area and delay count of basic block of Carry Select Adder (CSLA) is given in the following Table 1. [4], [6]

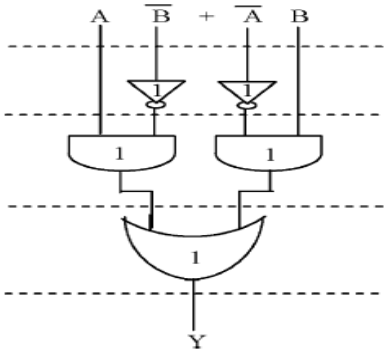

Fig1. *Delay and Area Evaluation of XOR gate*

Area and Delay Count of Basic Block of Carry Select Adder

Table1.

Adder blocks	Delay	Area
XOR	3	5
2:1 Mux	3	4
Half adder	3	6
Full adder	6	13

BINARY TO EXCESS1 CONVERTER

Binary to Excess-1 Converter (BEC) is combinational circuit formed by using XOR gate and AND gate [4]. The function of the Binary to Excess-1 converter is easily understandable by its functional Table 1.1. BEC is introduced in the conventional Carry Select Adder (CSLA) to make it faster in speed [6]. Also the replacement of one Ripple Carry Adder (RCA) having Cin = 1, with BEC makes reduction in the area of the circuit also. The Binary to Excess-1 converter logic of different bits can be designed using Boolean algebraic expressions. For the designing of 6-bit adder by using conventional Ripple Carry Adder, it requires six full adder and by evaluating the area it occupies 42 gates (7*6) and having delay of 36 (6*6), therefore when using BEC, it reduces area by 22 gates, i.e. 20 gates and delay of 30. For replacing n bit RCA, n+1 bit BEC circuitry is required.

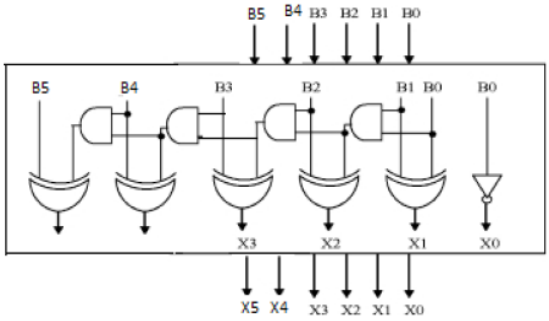

Fig2. *6-bit Binary to Excess1 Converter*

Functional Table of Binary to Excess1 Converter (BEC)

B [5:0]	X [5:0]
00000	**00001**
00001	**00010**
00010	**00011**
-	**-**
-	**-**
11111	**00000**

Boolean Expressions

X0 = ~B0;

X1 = B0 ^ B1;

X2 = B2 ^ (B0 & B1);

X3 = B3 ^ (B0 & B1 & B2);

X4 = B4 ^ (B0 & B1 & B2 & B3);

X5 = B5 ^ (B0 & B1 & B2 & B3 & B4);

REGULAR CARRY SELECT ADDER

In the carry propagation design, a carry select method is good comparatively in cost and performance from other adder circuits. The Carry Select Adder (CSLA) divides the adder circuit into several groups and each and every group performs additions in parallel. Therefore, there are dual Ripple Carry Adder (RCA) circuit, which act as carry evaluation block in each stage. One part evaluates the carry, assuming that Carry in is Zero, and other part evaluates when carry in is one.

When all carry signals are finally computed, then the final sum and carry out signal will be simply selected by 2:1 MUX. The major drawback of the conventional Carry Select Adder (CSLA) is the area cost which is double by using dual Ripple Carry Adder (RCA), i.e. another duplicate adder circuit evaluating with carry in one. A block diagram showing conventional Carry Select Adder using dual Ripple Carry Adder (RCA) and multiplexers in Fig.3

LOGICAL CONVERTER UNIT

In the proposed work, Logical Convertor Unit (LCU) is used in which gate level modification is done. Working of Logical Convertor Unit (LCU) is basically similar as Binary to Excess-1 Converter (BEC) given by Rajkumar and Kittur in 2012 [4]. The circuit is formed by using XOR gate and AND gate, therefore, by modifying the circuit by using basic gates AND, OR and NOT or Inverter (AOI) as proposed by P.Ramani in 2014 [1], redesigned the convertor by doing gate level modification and redefined as Logical Converter Unit (LCU), in such a way, so that it comparatively reduces delay and

area of the circuit so that redesigned Carry Select Adder (CSLA) functions faster. In the redesigned Carry Select Adder (CSLA), the input bits are given in linear way to achieve low power.

The main goal of Logical Converter Unit (LCU) is to provide lesser number of logic gates to attain reduced area and delay. The proposed study is implemented on 16-bit, 32-bit, 64-bit and 128-bit in Verilog using Xilinx 8.2i.

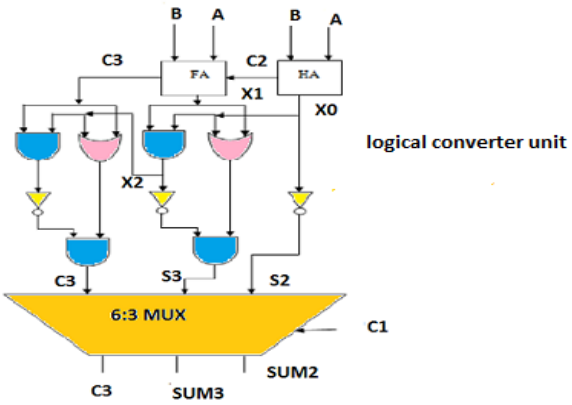

Fig3. *2-bit Block of CSLA using Logical Converter Unit*

Boolean Expression for LCU

S2 = ~X0;

S3 = (X0 + X1) & (X0 & X1);

C3 = (X0X2 + C2) & ~(X0X2C2);

RESULTS & CONCLUSION

Table2. *Delay and Area Count of Modified with Redesigned Carry Select Adder*

Bits	Delay in CSLA using BEC	Delay in CSLA using LCU	Area of CSLA using BEC	Area of CSLA using LCU
2 bit	13	8	43	40
3 bit	16	12	61	61
4 bit	19	16	84	82
5 bit	22	20	107	103

By redesigned Carry Select Adder by using logical converter unit (LCU), shows slightly reduction in the delay as well as area of the circuit. This implementation provides the faster response Carry Select Adder. The implementation of the adder circuit is done in the Verilog module using Xilinx 8.2i software and verify the simulation results. By comparing the Modified Carry Select Adder using BEC [4] with redesigned Carry Select Adder using Logical Converter Unit (LCU) we found that there is reduction of area and delay by 3.7% and 2.0%. This can be shown in the comparison table 2. The proposed work also makes the utilization of power less in small amount. The simulation result of 32-bit Carry Select Adder (CSLA) shown in fig. 4. The proposed study can also be implemented for 128 bits and 256 bits and will get good results.

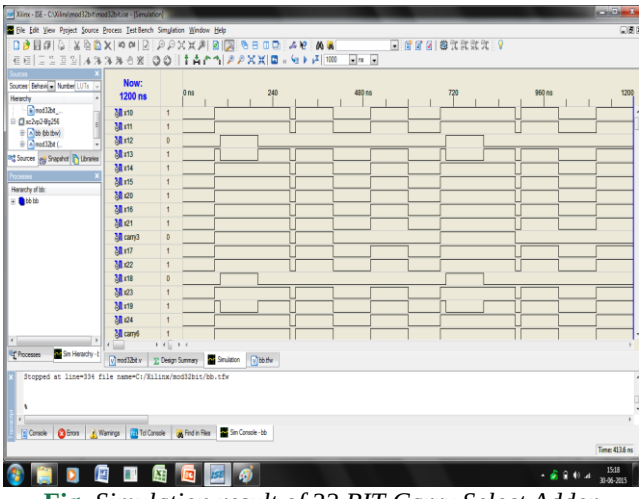

Fig. *Simulation result of 32 BIT Carry Select Adder*

REFERENCES

[1] P. Ramani, G. Priya, Murala Chandana, T. Sharmila, Seeram Tejasvi and M. Manjusri, "Low Power 256 – bit Modified Carry Select Adder", Research Journal of Applied Sciences, Engineering and Technology8(10): 1212 – 1216, September 2014 © Maxwell Scientific Organisation, 2014.

[2] Yajuan He, Chip-Hong Chang and Jiangmin Gu, "An Area Efficient 64-bit Square Root Carry Select Adder for Low Power Applications", 0-7803-8834-8/05, © IEEE 2005.

[3] Samiappa Sakthikumaran, S. Salivahanan, V.S Kanchana Bhaaskaran, V. Kavinilavu, B. Brindha and C. Vinoth in "A Very Fast and Low Power Carry Select Adder Circuit", 978-1-4244-8679-3/11, IEEE -2011.

[4] B.Ramkumar and Harish M Kittur, " Low Power and Area Efficient Carry Select Adder" IEEE transactions on Very Large Integration System (VLSI) VOL. 20, No. 2, February 2012.

[5] K Allipeera and S Ahmed Basha, "An Efficient 64-bit Carry Select Adder with Less Delay and Reduced Area Application" International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622, Vol. 2, Issue 5, Sept. – Oct. 2012, pp. 550 – 554.

[6] C. Sudarshan Babu and Dr. P. Ramana Reddy in "Implementation of 256 – bit high speed and area efficient Carry Select Adder", IJECET, Vol. 3, Issue 4, Oct. – Dec 2012.

[7] A. Nithyavel Krishna and C. Vijiya Bhaskar, "Low And Area Efficient of 128 bit Carry Select Adder" International Journal of Engineering Trends and Technology (IJETT) Vol. 5, No. 2, Nov. – 2013.

[8] T Y Chang and M J Hsiao, "Carry Select Adder using single Ripple Carry Adder" Electronics Letters 29th October 1998, Vol. 34 No. 2.

[9] Shipra Mishra and Shalendra Singh Tomar, "Design Low Power 10T Full Adder Using Process and Circuit Techniques", Proceedings of 7th International Conference on Intelligent Systems and Control (ISCO 2013), ©IEEE 2012.

[10] M. Chihra and G. Omkareshwari, "128-bit Carry Select Adder Having Less Area and Delay", International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, Vol. 2, Issue 7, July 2013.

[11] Patel Chandransh and C.S. Veena,"Ripple Carry Adder Design Using Universal Logic Gates", Research Journal of Engineering Sciences, ISSN – 2278 – 9472, Vol. 3(11), November 2014, pp – 1-5.

[12] K. Swarnlatha, S.Mohan Das and P.Uday Kumar, "An Efficient Carry Select Adder With Less Delay and Reduced Area Using FPGA QUARTUS II Verilog Design", International Journal of Sciences, Engineering and Technology Research (IJSETR), Vol. 2, Issue 8, August 2013.

[13] K Saranya, "Low Power and Area Efficient Carry Select Adder", International Journal of Soft Computing and Engineering (IJSCE), Vol. 2, Issue 6, January 2013.

[14] Prof. Mary Joseph and Renji Narayanan, "16 Bit Carry Select Adder with Low Power and Area", International Journal on Recent and Innovation Trends in Computing and Communication (IJRITCC), Vol. 2, Issue 5, May 2014.

[15] Pallavi Saxena, Urvashi Purohit and Priyanka Joshi, "Analysis of Low Power, Area-Efficient and High Speed Fast Adder", International Journal of Advanced Research in Computer and Communication Engineering (IJARCCE), Vol. 2, Issue 9, September 2013.

[16] R.Uma, Vidya Vijayan, M.Mohanapriya and Sharon Paul, "Area, Delay and Power Comparison of Adder Topologies", International Journal of VLSI Design & Communication Systems (VLSICS), Vol. 3, No. 1, February 2012.

[17] Mr. P.C.Samual Joshua and Mr. P.C.Praveen Kumar, "512-Bit Implementation of Area Efficient and High Speed Carry Select Adder", International Journal of Scientific Engineering and Technology Research (IJSETR), Vol. 2, Issue 7, July 2013, Page no. 487 – 493.

[18] Saraswati, "128-Bit Area Efficient Carry Select Adder", International Journal for Technological Research in Engineering, Vol. 1, Issue 9, May 2014.