

Implementation of Convolution Encoder and Adaptive Viterbi Decoder for Error Correction

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ABSTRACT

Cyclic codes are also called cyclic redundancy check (CRC) codes primarily used today for the error detection applications rather than for error correction. All communication channels are subject to the additive white Gaussian noise (AWGN) around the environment. Forward error correction (FEC) techniques are used in the transmitter to encode the data stream and receiver to detect and correct bits in errors, hence minimize the bit error rate (BER) to improve the performance. RS decoding algorithm Due to weaknesses of using the block codes for error correction in useful channels, another approach of coding called Convolutional coding had been introduced in 1955. Convolutional encoding with Viterbi decoding is a powerful FEC technique that is particularly suited to a channel in which the transmitted signal is corrupted mainly by AWGN. It operates on data stream and has memory that uses previous bits to encode. It is simple and has good performance with low implementation cost. The Viterbi algorithm (VA) was proposed in 1967 by Andrew Viterbi and is used for decoding a bit stream that has been encoded using FEC code. The Convolutional encoder adds redundancy to a continuous stream of input data by using a linear shift register. This paper is Convolutional encoder and adaptive Viterbi decoder (AVD) with a constraint length, Kis implemented using Verilog and Xilinx 13.2 tool.

Keywords: crc, hamming codes, encoder, decoder.

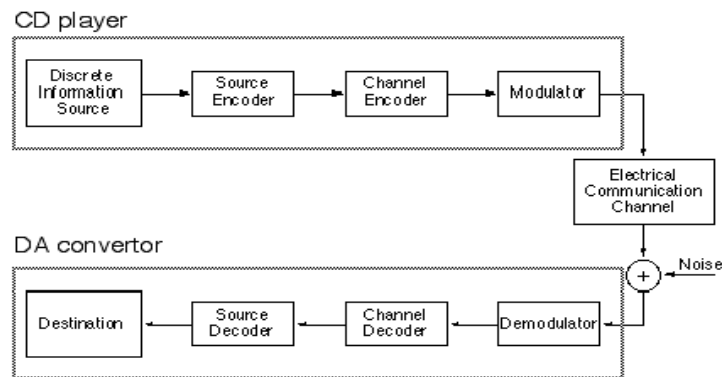
INTRODUCTION

Digital communication system is used to transport an information bearing signal from the source to a user destination via a communication channel. The information signal is processed in a digital communication system to form discrete messages which makes the information more reliable for transmission. Channel coding is an important signal processing operation for the efficient transmission of digital information over the channel. It was introduced by Claude E.Shannon in 1948 by using the channel capacity as an important parameter for error free transmission. In channel coding the number of symbols in the source encoded message is increased in a controlled manner in order to facilitate two basic objectives at the receiver: error detection and error correction. Error detection and error correction to achieve good communication is also employed in electronic devices. It is used to reduce the level of noise and interferences in electronic medium. The amount of error detection and correction required and its effectiveness depends on the signal to noise ratio (SNR).In source coding, the encoder maps the digital generated at the source output into another signal in digital form. The objective is to eliminate or reduce redundancy so as to provide an efficient representation of the source output. Since the source encoder mapping is one-to –one, the source decoder on the other end simply performs the inverse mapping, thereby delivers to the user a reproduction of the original digital source output. The primary benefit thus gained from the application of source coding is a reduced bandwidth requirement.In channel coding, the objective for the encoder is to map the incoming digital signal into a channel input and for the decoder is to map the channel output into an output signal in such a way that the effect of channel noise is minimized. That is the combined role of the channel encoder and decoder is to provide for a reliable communication over a noisy channel. This provision is satisfied by introducing redundancy in a prescribed fashion in the channel encoder and exploiting it in the decoder to construct the original encoder input as accurately as possible. Thus in source coding, redundant bits are removed whereas in channel coding, redundancy is introduced in a

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controlled manner. Then modulation is performed for the efficient transmission of the signal over the channel. Various digital modulation techniques could be applied for modulation such as Amplitude Shift Keying (ASK), Frequency- Shift Keying (FSK) or Phase – Shift Keying (PSK).



Hamming Codes

In telecommunication, Hamming codes are a family of linear error-correcting codes that generalize the Hamming (7,4)-code invented by Richard Hamming in 1950. Hamming codes can detect up to two-bit errors or correct one-bit errors without detection of uncorrected errors. By contrast, the simple parity code cannot correct errors, and can detect only an odd number of bits in error. Hamming codes are perfect codes, that is, they achieve the highest possible rate for codes with their block length and minimum distance of three. In mathematical terms, Hamming codes are a class of binary linear codes. For each integer $r \geq 2$ there is a code with block length $n = 2r - 1$ and message length $k = 2r - r - 1$. Hence the rate of Hamming codes is $R = k / n = 1 - r / (2r - 1)$, which is the highest possible for codes with minimum distance of three (i.e., the minimal number of bit changes needed to go from any code word to any other code word is three) and block length $2r - 1$. The parity-check matrix of a Hamming code is constructed by listing all columns of length r that are non-zero, which means that the dual code of the Hamming code is the punctured Hadamard code. The parity-check matrix has the property that any two columns are pair wise independent. Due to the limited redundancy that Hamming codes add to the data, they can only detect and correct errors when the error rate is low. This is the case in computer memory (ECC memory), where bit errors are extremely rare and Hamming codes are widely used. In this context, an extended Hamming code having one extra parity bit is often used. Extended Hamming codes achieve a Hamming distance of four, which allows the decoder to distinguish between when at most one one-bit error occurs and when any two-bit errors occur. In this sense, extended Hamming codes are single-error correcting and double-error detecting, abbreviated as SECDED

The following general algorithm generates a single-error correcting (SEC) code for any number of bits.

- Number the bits starting from 1: bit 1, 2, 3, 4, 5, etc.
- Write the bit numbers in binary: 1, 10, 11, 100, 101, etc.
- All bit positions that are powers of two (have only one 1 bit in the binary form of their position) are parity bits: 1, 2, 4, 8, etc. (1, 10, 100, 1000)
- All other bit positions, with two or more 1 bits in the binary form of their position, are data bits.
- Each data bit is included in a unique set of 2 or more parity bits, as determined by the binary form of its bit position.
 - Parity bit 1 covers all bit positions which have the least significant bit set: bit 1 (the parity bit itself), 3, 5, 7, 9, etc.
 - Parity bit 2 covers all bit positions which have the second least significant bit set: bit 2 (the parity bit itself), 3, 6, 7, 10, 11, etc.

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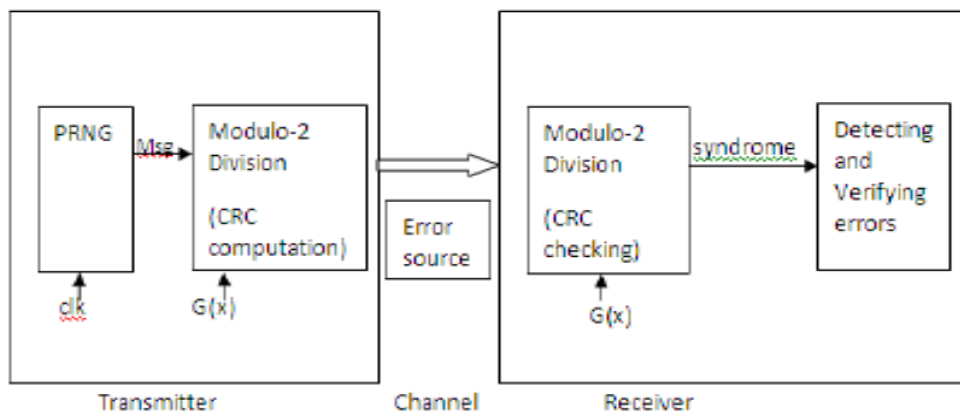
- Parity bit 4 covers all bit positions which have the third least significant bit set: bits 4–7, 12–15, 20–23, etc.
- Parity bit 8 covers all bit positions which have the fourth least significant bit set: bits 8–15, 24–31, 40–47, etc.
- In general each parity bit covers all bits where the bitwise AND of the parity position and the bit position is non-zero.

(7, 4) Hamming Code

p_0	p_1	u_3	p_2	u_2	u_1	u_0
1	2	3	4	5	6	7

Information	1 p_0	2 p_1	3 u_3	4 p_2	5 u_2	6 u_1	7 u_0
0	0	0	0	0	0	0	0
1	1	1	0	1	0	0	1
2	0	1	0	1	0	1	0
3	1	0	0	0	0	1	1
4	1	0	0	1	1	0	0
5	0	1	0	0	1	0	1
6	1	1	0	0	1	1	0
7	0	0	0	1	1	1	1
8	1	1	1	0	0	0	0
9	0	0	1	1	0	0	1
10	1	0	1	1	0	1	0
11	0	1	1	0	0	1	1
12	0	1	1	1	1	0	0
13	1	0	1	0	1	0	1
14	0	0	1	0	1	1	0
15	1	1	1	1	1	1	1

Communication Using CRC Error Detection Algorithm



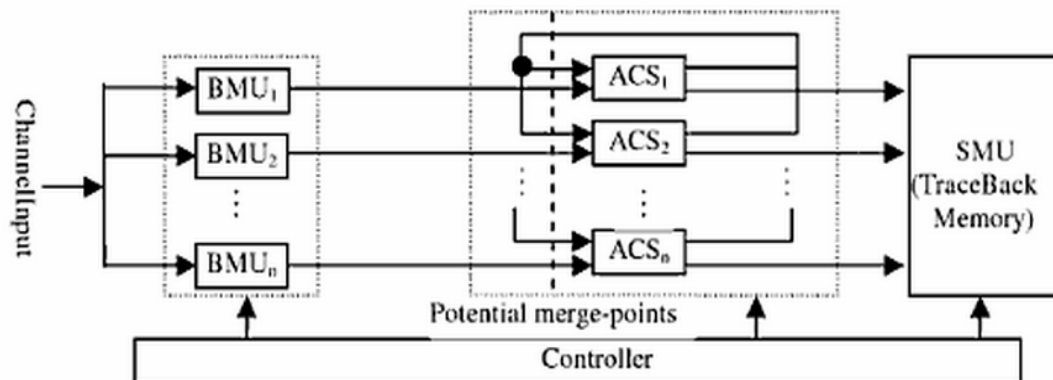
The communication application using CRC as error detection algorithm. The PRNG – Pseudo Random Number Generator Is used to generate 8 bit messages $d(x)$. The Transmitter will perform CRC computation to encode the message by adding checksum value to it. This encoded message is called codeword $c(x)$. The channel is unreliable transmission line which may corrupt the message due to noise, attenuation and interference. The possibly corrupted codeword at the receiver is decoded using CRC checking algorithm. Note that transmitter and receiver agrees on common generator polynomial $G(x)$. The result of CRC checking is called Syndrome $s(x)$ is used to detect error in the received message. A cyclic code can be analyzed to find its capabilities by using

polynomials. Message: $d(x)$ Codeword: $c(x)$ Generator: $g(x)$ Syndrome: $s(x)$ Error: $e(x)$ in this analysis the intention is to find the criteria that must be imposed on the generator, $G(x)$ to detect the type of error. Here, received codeword = $c(x) + e(x)$ the receiver divides the received codeword by $g(x)$ to get the syndrome. This can be written as: Received codeword = $c(x) + e(x)$ the first term does not have remainder. The second term does not have a remainder (syndrome = 0), in two cases the first case when $e(x)$ is 0 if there is no error. The second case when $e(x)$ is divisible by $G(x)$. Those errors that are divisible by $g(x)$ are not caught. In a cyclic code, those $e(x)$ errors that are divisible by $g(x)$ are not caught.

Block Diagram of Viterbi Algorithm

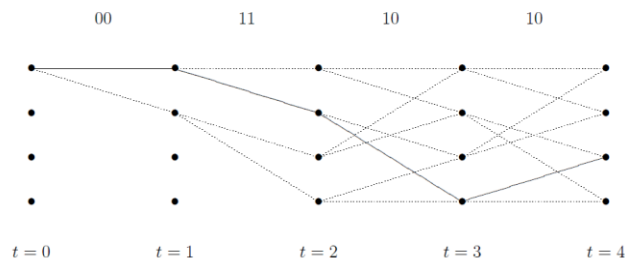
The Viterbi algorithm is one of the standard sections in number of high-speed modems of the process for information infrastructure applicable in modern world. The dynamic algorithm includes some path metrics so as to compute the path sequence transmitted earlier the name Viterbi algorithm arrived after Andrew Viterbi and is represented as VA for reorganization, record of huge possibility decodes as well as least reserved decoding are generally similar in a defined binary symmetric channel. Kia, J. (2005, p.1) explains Viterbi algorithm as a “dynamic algorithm that uses certain path metrics to compute the most likely path of a transmitted sequence” [13]. The basic performance of the Viterbi decoder is analyzed with the block diagram shown below. It consists of three main blocks branch metric unit, add compare select and trace back unit. The unit of branch metric will calculate all the branch metrics and then processed to add compare for selecting the surviving branches as per the branch metrics finally the decoded data bits are generated by the trace back unit. The overall performance of the Viterbi algorithm is analyzed with the help of conventional codes. The simulated block diagram explains the operation of detecting and correcting the coding errors in normal communication system.

The Basic Block Diagram of Viterbi Decoder



The transmitted bits of data are encoded in the first block with conventional code that is (CC encoder) which are modulated by means of binary pulse-amplitude modulation (PAM) so as to tune those bits into antipodal bits and process to the additive white Gaussian noise (AWGN) channel thus obtained data combined with noise is supplied to soft decision Viterbi algorithm (SDVA) which only accepts the antipodal data at the input for decoding and produces the output decoded bits. Implementation of the Viterbi algorithm is supported with two main steps the initial step is to select the trellis from the bits that are achieved at the input at the receiver. A simple trellis figure shows with four stage points for transmission, each state is represented with a dot and the state transition is shown as edge of branch. Each and every branch is known as the branch metric as it is associated at Euclidean distance with the symbol towards final transition.

Viterbi Algorithm Trellis



For calculating the branch metric can be obtained with the trellis using the Euclidean analysis as follows:

$$\begin{aligned}
 \text{BM}(r_r, b_b) &= (r_0 - b_0)^2 + (r_1 - b_1)^2 \\
 &= r_0^2 - 2r_0b_0 + b_0^2 + r_1^2 - 2r_1b_1 + b_1^2 \\
 &= r_0b_0 + r_1b_1
 \end{aligned}$$

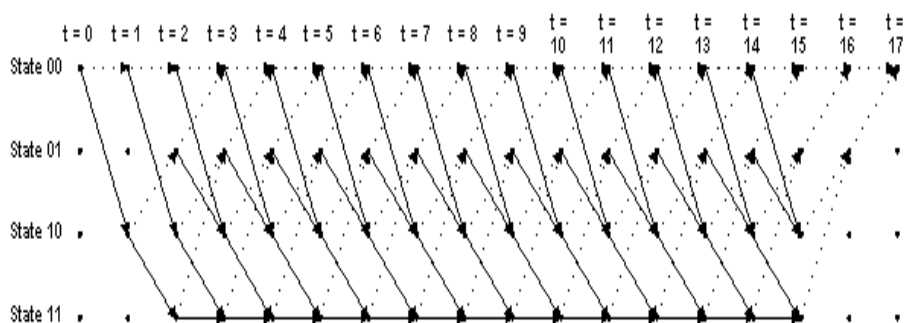
Where,

RR = symbol received at the input

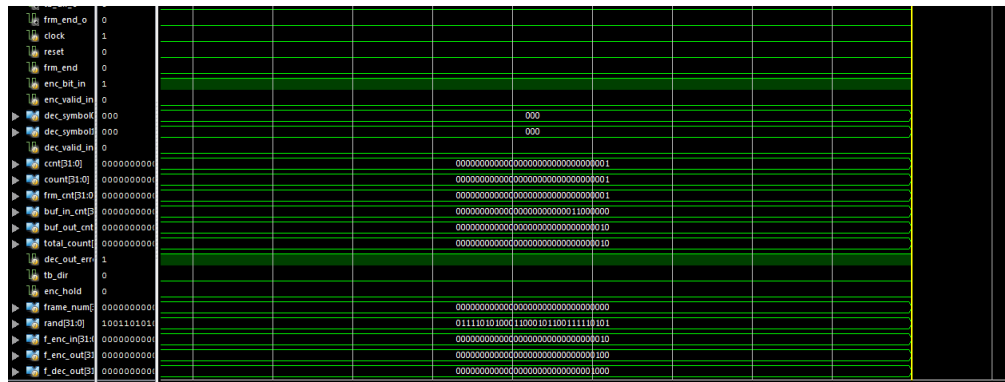
Bs = branch symbol

Both RR and bs are dependent on the used for conventional encoder. Under the basic assumption that there is no noise in the data and the value of r and b will vary between -1 to +1, the range of branch metric will range within -2 to +2. In case $r_r = b_b$ branch metric would be 2, Similarly $r_0 = -b_0$ as well as $r_1 = -b_1$ and $\text{BM} = -2$. The path metric (λ) in the minimum Euclidean distance in the trellis does not required the actual value the original order of the floating point pair numbers is $\lambda_{\text{new}} = \lambda_{\text{prev}} + r_0b_0 + r_1b_1$. The path metric λ is the shortest distance among cumulative state, thus distance of the path (Euclidean distance) is inversely proportional to the branch metric. After complication of generating a trellis it is necessary to find survivor path with maximum path metric. In the above the solid black line is the survivor path. Viterbi algorithm is basically implemented to decode the errors found in convolution encoded sequence. As discussed the Viterbi algorithm will make use of trellis structure in finding the coded sequence based on the transmission signals. Since each and every code sequence will follow based on the trellis process of encoding data. Considering an example of trellis diagram of half rate, three convolution encoder $K=3$ and 15 bit messages with four possible states shown in 4 horizontal rows with dots. 18 columns shows the time instants from t_0 to t_{17} both $t=0$ and $t=17$ has the four dot column which is initial and final state situations while encoding messages. The state transition is shown with a dotted line at zero input. The figure shows the state of trellis, which reach the encoding of messages.

Trellis Diagram of Viterbi Algorithm



SIMULATION RESULTS



CONCLUSION

The Convolutional encoder and adaptive Viterbi decoder are implemented. This design has been simulated and synthesized using XILINX-ISE 13.2 The given input sequence has been encoded by using Convolutional encoder and it is transmitted through the channel. Finally, the transmitted sequence is decoded by the Viterbi decoder and the estimated original sequence is produced.

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