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High Speed and Low Power Multiplier Using Reversible Logic for Wireless Communications

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ABSTRACT

Multipliers are vital components of any processor or computing machine, performance of microcontrollers and Digital signal processors are evaluated on the basis of number of multiplications performed in unit time. Hence better multiplier architectures are bound to increase the efficiency of the system. Vedic multiplier is one such promising solution. It's simple architecture coupled with increased speed forms an unparalleled combination for serving any complex multiplication computations. Tagged with these highlights, implementing this with reversible logic further reduces power dissipation. Power dissipation is another important constraint in an embedded system which cannot be neglected. In this paper we bring out a Vedic multiplier known as "Urdhva Tiryakbhayam" meaning vertical and crosswise, implemented using reversible logic vedic multiplier with 4,8,16,32 bit sizes.

Keywords: Reversible logic, Urdhva Tiryakbhayam..

INTRODUCTION

Vedic mathematics [I] is the ancient Indian system of mathematics which mainly deals with Vedic mathematical formulae and their application to various branches of Mathematics. Vedic mathematics was reconstructed from the ancient Indian scriptures (Vedas) by Sri Bharati Krsna Tirtha after his research on Vedas [16]. He constructed 16 sutras and 16 upa sutras after extensive research in Atharva Veda. The most famous among these 16 are Nikhilam Sutram, Urdhva Tiryakbhayam, and Anurupye. It has been found that Urdhva Tiryakbhayam is the most efficient among these. The beauty of Vedic mathematics lies in the fact that it reduces otherwise cumbersome looking calculations in conventional mathematics to very simple ones. This is so because the Vedic formulae are claimed to be based on the natural principles on which the human mind works. Hence multiplications in DSP blocks can be performed at faster rate. This is a very interesting field and presents some effective algorithms which can be applied to various branches of engineering. Digital signal processing (DSP) is the technology that is omni present in almost every engineering discipline. Faster additions and multiplications are the order of the day. Multiplication is the most basic and frequently used operations in a CPU. Multiplication is an operation of scaling one number by another. Multiplication operations also form the basis for other complex operations such as convolution, Discrete Fourier Transform, Fast Fourier Trans forms, etc. With ever increasing need for faster clock frequency it becomes imperative to have faster arithmetic unit. Hence Vedic mathematics can be apply employed here to perform multiplication. Reversible logic is one of the promising fields for future low power design technologies. Since one of the requirements of all DSP processors and other hand held devices is to minimize power dissipation multipliers with high speed and lower dissipations are critical. This paper proposes an implementation of Reversible Urdhva Tiryakbhayam Multiplier which consists of two cardinal features. One is the fast multiplication feature derived from Vedic algorithm Urdhva Tiryakbhayam and another is the reduced heat dissipation by the virtue of implementing the circuit using reversible logic gates.

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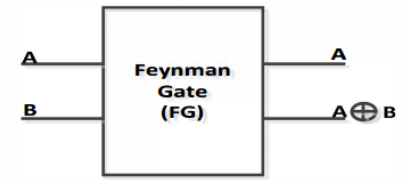
REVERSIBLE LOGIC

Reversible logic is a promising computing design paradigm which presents a method for constructing computers that produce no heat dissipation. Reversible computing emerged as a result of the application of quantum mechanics principles towards the development of a universal computing machine. Specifically, the fundamentals of reversible computing are based on the relationship between entropy, heat transfer between molecules in a system, the probability of a quantum particle occupying a particular state at any given time, and the quantum electrodynamics between electrons when they are in dose proximity. The basic principle of reversible computing is that a objective device with an identical number of input and output lines will produce a computing environment where the electrodynamics of the system allow for prediction of all future states based on known past states, and the system reaches every possible state, resulting in no heat dissipation. A reversible logic gate is an N-input N-output logic device that provides one to one mapping between the input and the output. It not only helps us to determine the outputs from the inputs but also helps us to uniquely recover the inputs from the outputs. Garbage outputs are those which do not contribute to the reversible logic realization of the design. Quantum cast refers to the cost of the circuit in terms of the cost of a primitive gate. Gate count is the number of reversible gates used to realize the function. Gate level refers to the number of levels which are required to realize the given logic functions. The following are the important design constraints for reversible logic circuits. Reversible logic gates do not allow fan-outs. Reversible logic circuits should have minimum quantum cost. The design can be optimized so as to produce minimum number of garbage outputs. The reversible logic circuits must use minimum number of constant inputs. The reversible logic circuits must use a minimum logic depth or gate levels. The basic reversible logic gates encountered during the design are listed below:

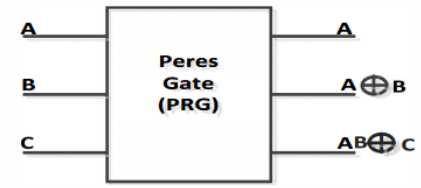
Feynman Gate

It is a 2x2 gate and its logic circuit is as shown in the figure. It is also known as Controlled Not (CNOT) Gate. It has quantum cost one and is generally used for Fan Out purposes.



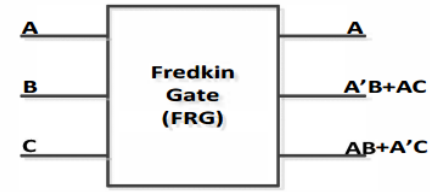
Peres Gate

It is a 3x3 gate and its logic circuit is as shown in the figure. It has quantum cost four. It is used to realize various Boolean functions such as AND, XOR.



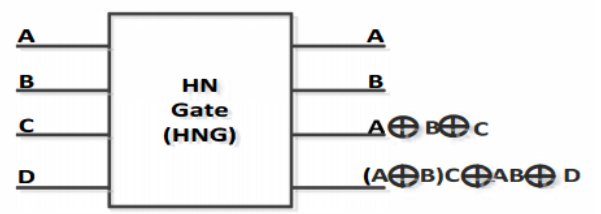
Fredkin Gate

It is a 3x3 gate and its logic circuit is as shown in the figure. It has quantum cost five. It can be used to implement a Multiplexer.



HNG Gate

It is a 4x4 gate and its logic circuit is as shown in the figure. It has quantum cost six. It is used for designing ripple carry adders. It can produce both sum and carry in a single gate thus minimizing the garbage and gate counts.

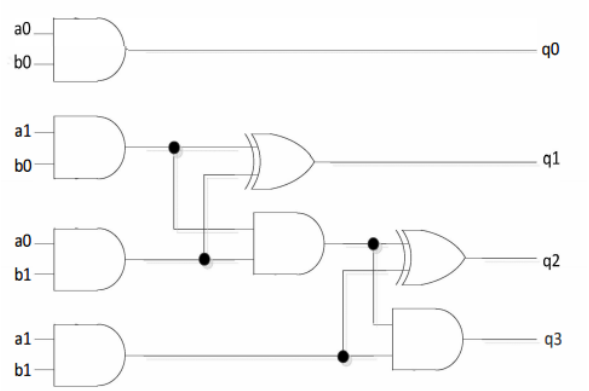


Urdhva Tiryakbhayam

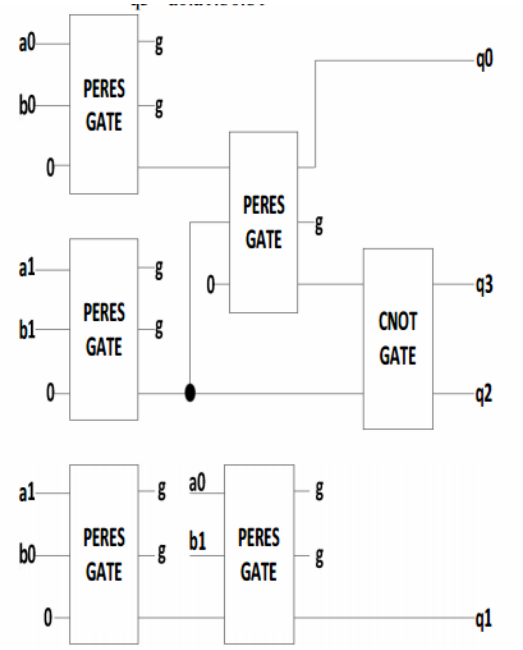
Urdhva Tiryakbhayam (UT) is a multiplier based on Vedic mathematical algorithms devised by ancient Indian Vedic mathematicians. Urdhva Tiryakbhayam sutra can be applied to all cases of multiplications viz. Binary, Hex and also Decimals. It is based on the concept that generation of all partial products can be done and then concurrent addition of these partial products is performed. The parallelism in generation of partial products and their summation is obtained using Urdhva Tiryakbhayam. Unlike other multipliers with the increase in the number of bits of multiplicand and/or multiplier the time delay in computation of the product does not increase proportionately. Because of this fact the time of computation is independent of c10ck frequency of the processor. Hence one can limit the clock frequency to a lower value. Also, since processors using lower clock frequency dissipate lower energy, it is economical in terms of power factor to use low frequency processors employing fast algorithms like the above mentioned. The Multiplier based on this sutra has the advantage that as the number of bits increases, gate delay and area increases at a slow pace as compared to other conventional multipliers. The algorithm can be iIlustrated using the following visual walkthrough. Figure shows the application of the algorithm for decimal multiplication and for binary multiplication.

REVERSIBLE URDHVA TIRYAKBHAAM MULTIPLIER

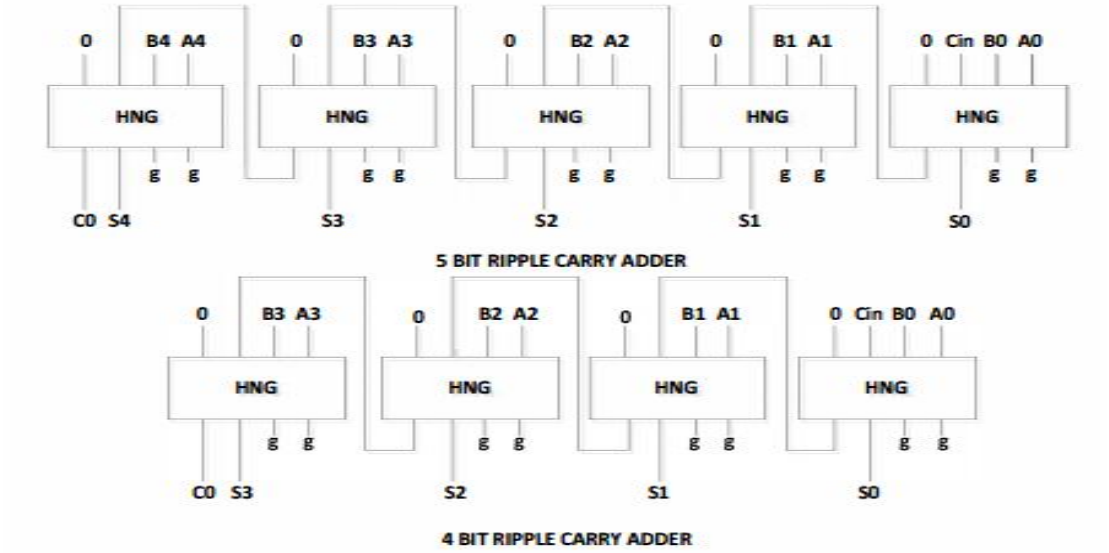
The digital logic implementation of the 2X2 Urdhva Tiryakbhayam multiplier using the conventional logic gates is as shown in figure. The expressions for the four output bits are given under. This design does not consider the fan-out. The circuit requires a total of six reversible logic gates out of which five are Peres gates and remaining one is the Feynman Gate. The quantum cost of the 2X2 Urdhva Tiryakbhayam Multiplier is enumerated to be 21. The number of garbage outputs is 9 and number of constant inputs is 4.



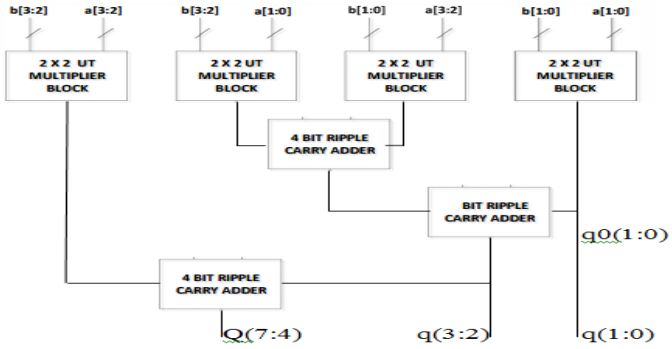
The Reversible Implementation



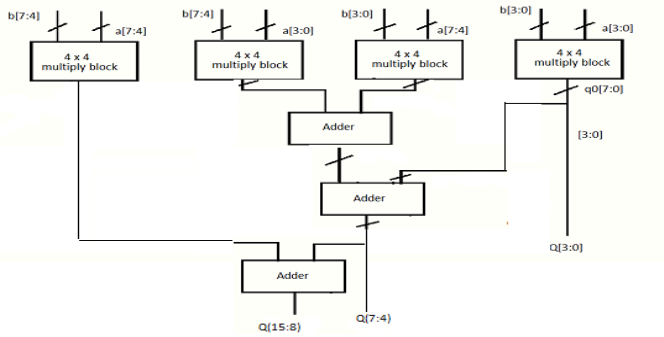
The Reversible 4X4 Urdhva Tiryakbhayam Multiplier design from the 2X2 multiplier. The block diagram of the 4X4 Vedic Multiplier is presented in the figure It consists of four 2X2 multipliers each of which procedures four bits as inputs; two bits from the multiplicand and two bits from the multiplier. The lower two bits of the output of the first 2X2 multiplier are entrapped as the lowest two bits of the final result of multiplication. And second multiplier output ,third multiplier output given as input to the four bit ripple carry adder then get output. Adder output and first multiplier output add three zeros are given as input to five input bits ripple carry adder then get output. Adder output and fourth multiplication given as input four bit ripple carry adder. These six bits from the upper bits of the final result. The ripple carry adder is consummated (realized) using the HNG Gate. The number of bits that need to be ripple carried verdicts the number of HNG gates to be used. Thus a 4 bit ripple carry adder needs 4 HNG gates and the 5 bit adder requires 5 HNG gates. This design also does not take into consideration the fan out gates. For this design the quantum cost is computed to be 162, the total number of gates used will be 37, the number of garbage outputs will be 62 and the number of constant inputs will be 29.



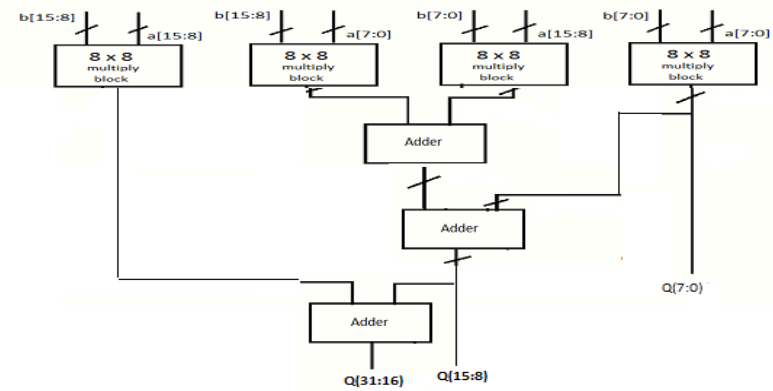
4x4 Multiplier



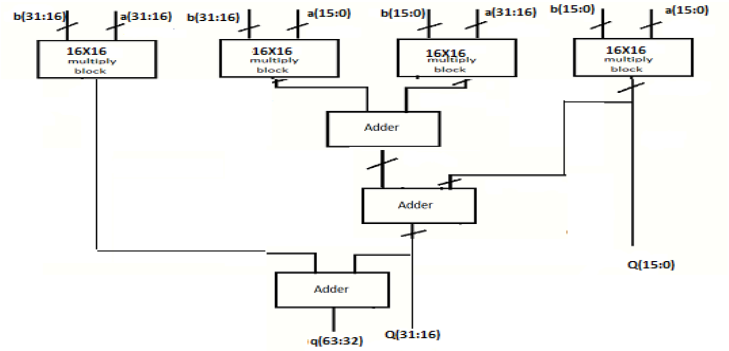
8x8 Multiplier



16x16 Multiplier

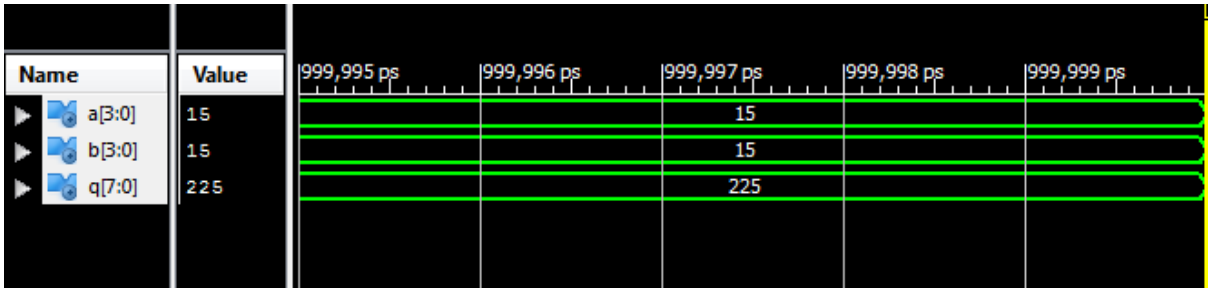


32x32 Multiplier

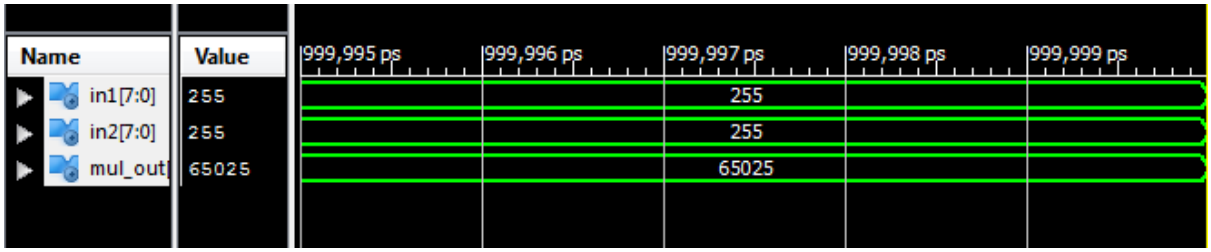


SIMULATION RESULTS

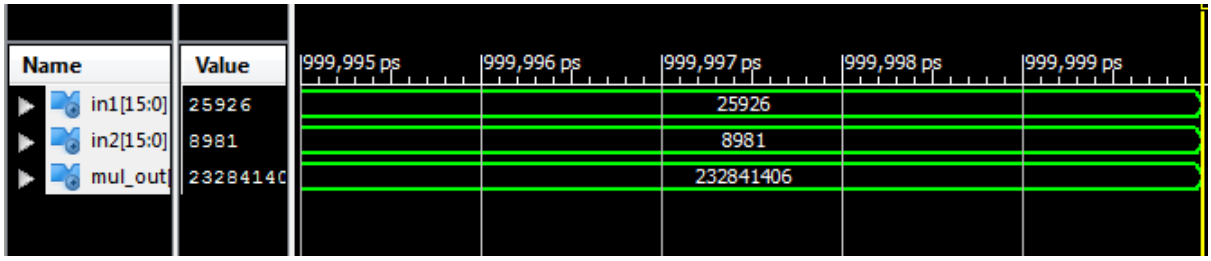
4x4 Multiplier



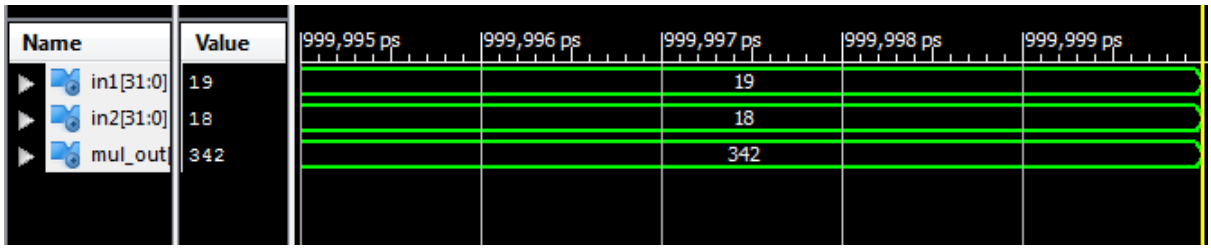
8x8 Multiplier



16x16 Multiplier



32x32 Multiplier



CONCLUSION

The Urdhva Tiryakbhayam Vedic Multiplier realized using reversible logic gates. Firstly a basic 2x2 UT multiplier is designed. This design stems from the conventional logic implementation. After this, the 2x2 UT multiplier block is cascaded to obtain 4x4 multiplier. The 4x4 UT multiplier block is cascaded to obtain 8x8 multiplier. The 8x8 UT multiplier block is cascaded to obtain 16x16 multiplier. The 16x16 UT multiplier block is cascaded to obtain 32x32 multiplier The ripple carry adders which were required for adding the partial products were constructed using HNG gates.4 bit vedic multiplier designed and get simulation and synthesis waveforms using Xilinx 13.2.

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